2009 Technology Plan Reviews - Introduction

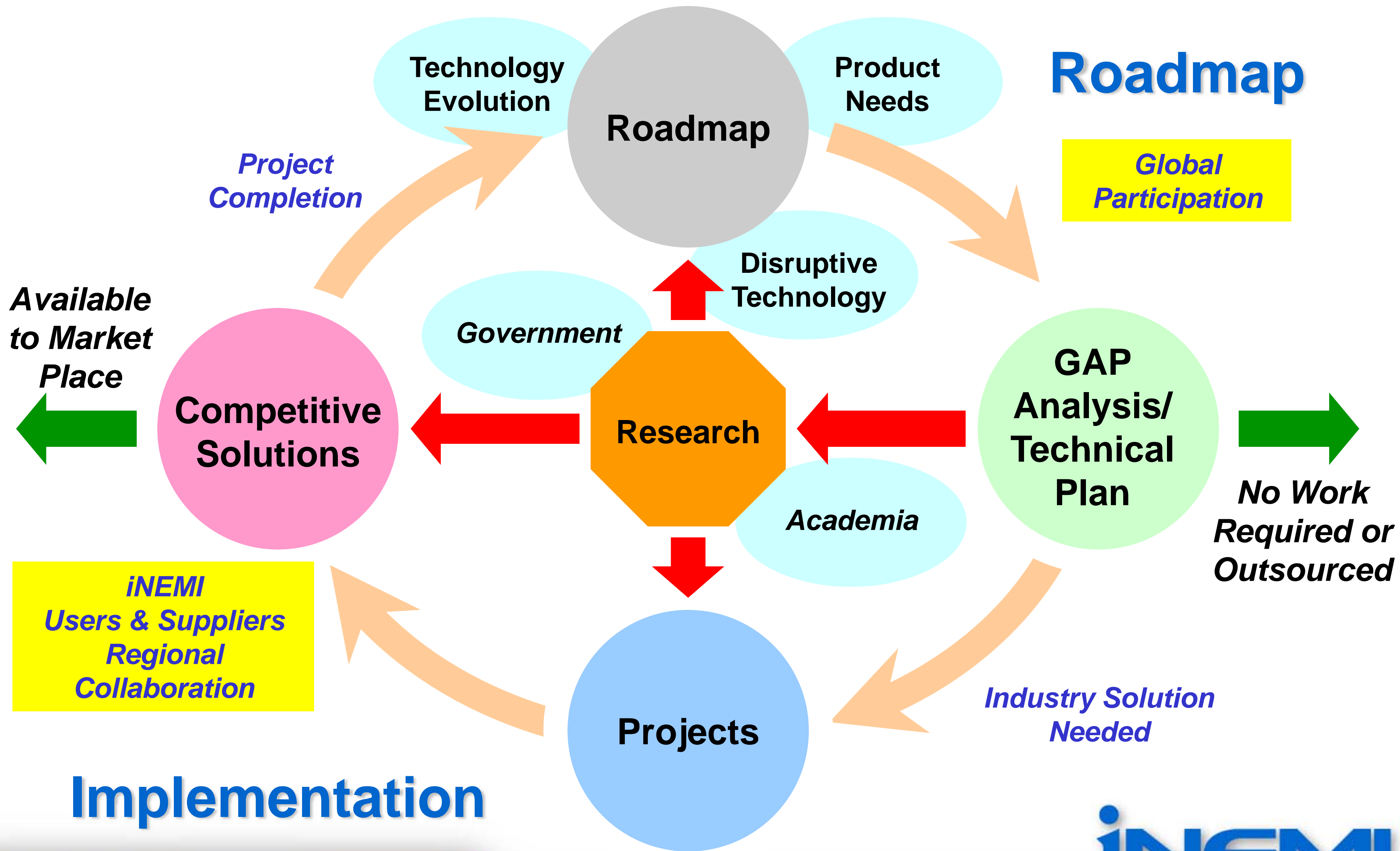
April 3, 2009
Chuck Richardson

Advancing manufacturing technology

TIG Chair Technical Plan Agenda

TIME:	TOPIC:	DISCUSSION LEADER:
7:30 AM	Breakfast	
7:45 AM	Introduction and Review of Agenda:	Bob Pfahl
7:55 AM	Overview of 2009 Technical Plan & Research Priorities	Chuck R
8:10 AM	Technical Plan-Board Assembly	Ian Williams
8:30 AM	Technical Plan- Organic Packaging Substrates	Hamid Azimi
8:50 AM	Technical Plan- Board & Systems Mfg. Test	Rosa Reinosa
9:10 AM	Technical Plan- Organic PCB	John Davignon
9:30 AM	Break	
9:40 AM	Technical Plan- Medical Electronics	Tony Primavera
10:00 AM	Technical Plan-Environmentally Conscious Electronics	Scott O'Connell
10:20 AM	Technical Plan-Optoelectronics	Brian Roche
10:30 AM	Discussion and Action Plan	All
10:50 AM	TC Business Meeting	
12:00 PM	Close	

Methodology



iNEMI

Roadmap Chapter Reviews-2009

Roadmap TWGs	TC Reviewer	Gap Analysis	Applicable TIGs	Identified Gap Descriptions
Large Area, Printed Electronics	Aroon Tungare			Categorization of Semiconducting Inks
Information Management	Barbara G.		Information Management	Supply Chain Information Exchange
Modeling, Simulation, and Design	Jie Xue			Business Model for DFx / Outsource
Thermal Management	Jim Arnold		Thermal Management	Dissipation of Increasing Point Source Power Loads
Environmentally Conscious Electronics	Mike Davisson	APEX	ECE	Environmental Compliance/Sustainability Issues
Board Assembly	Peter Tomaiuolo	APEX	Board Assembly	Lead Free Issues - Wave, Rework, DfX
Test, Inspection & Measurement	Michael Roesch	APEX	Board & Systems Mfg. Test	Test Access Issues
Final Assembly.	Koen Gieskes			Design Standards; Define Processes/Functions
Packaging	Mario Bolanos Avila		Packaging Reliability	R&D Funding, Environmental Issues, Process Diversity, Reliability
Interconnection Substrates - Organic	Mostafa Aghazadeh	APEX	Organic Packaging Substrates	Low Cost, High Density Advances
Interconnection Substrates - Organic	Mostafa Aghazadeh	APEX	Organic PCB	Low Cost, High Density Advances, HFR-free Issues
Interconnection Substrates - Ceramic	Bob Pfahl		Substrates	Standards, Training For LTTC
Passive Components	Sunny Liu			Assembly of 01005 Discretes, Lead Free Temperatures
RF Components & Subsystems	Jie Xue			Commercial Infrastructure For Antennas, Filters, etc.
Optoelectronics	Peter T.		Optoelectronics	Low Cost Components
Photovoltaics	Carol Handwerker			Higher Efficiency Materials, Lower Cost Per Watt
Connectors	Rob Rix		Connectors	High Speed, Opto Connectors/Cables
Solid State Illumination	Alan Rae			Lower Cost Products
Mass Data Storage	Sherwin Kahn			Continue Reducing Cost Per Bit
Medical	Bill Barthel	APEX	Medical	Improve Remote Patient Capabilities

Red Background Denotes Retired 2007 TIG

Yellow Background Denotes Potential 2009 TIG

Green Background Denotes Approved TIG For 2009

Current Tasks

- TIG Chairs to Hold Gap Analysis Meetings at APEX / Possible ECE TIG Gap Analysis Meeting at ISSST in Phoenix, Arizona 5/19-21/09
- TIG Chairs / TC Discuss Gaps At APEX 4/3/09
- TIG Chairs / Staff Develop Technical Plan From Analysis Meetings and T.C. Feedback From APEX Meeting
- T.C. and R.C. Face to Face Meetings on Technical Plan and Research Priorities Drafts / Status 5/26-29/09 ECTC, San Diego
- TIGs Finalize Their Plans Based on T.C. Feedback 7/15/09
- Research Committee Face to Face to Review Research Priorities Draft 7/?/09
- Release 2007 Technical Plan / Research Priorities 8/15/09

OFC / APEX TIG / TC Meetings

Monday, March 23	Optoelectronics TIG Gap Analysis
11:00 – 12:00 Noon	
Tuesday, March 31	
9:00 a.m. – 10:00 am	Board & Systems Mfg. Test TIG Gap Analysis
Wednesday, April 1	
8:00 am – 10:00 am	Board Assembly TIG Gap Analysis
10:00 am – 12:00 pm	ECE TIG Gap Analysis
10:00 am – 12:00 pm	Organic PCB TIG Gap Analysis
1:00 pm – 3:00 pm	Organic Packaging Substrates TIG Gap Analysis
5:00 pm – 8:00 pm	Medical TIG Gap Analysis
Thursday, April 2	
6:30 – 9:00 p.m.	TC / TIG Chair Dinner at Excaliber
Friday, April 3	
7:30 am – 10:50 am	TIG Chair/TC Technical Plan Review

Technical Plan Template

CONCEPT

- 2009 Roadmap is the Strategy Document
- GAP Analysis is foundation for Technical Plan
- Technical Plan = Implementation Plan

Technical Plan Template

- Outline for each TIGs Technical Plan input
  - Introduction
  - Gap Analysis and Five-year plan
  - What has changed
  - TIG Plan
    - Projects/programs to focus on short term -prioritize
    - Identify areas where research is needed -prioritize
  - Summary

Introduction

- **Scope: Defines TIG responsibility**

- **Background: This is a brief set of statements on what this TIG's technical plan contains, how it was developed, and any other pertinent information.**

Five-year Plan

- The 5-year plan chart (See example next chart) is the heart of the Technical Plan. It is a visualization of all steps in the Manufacturing Process covered by the TIG indicating by what year the technologies need to be deployed to realize the product sector requirements per the 2009 technology roadmap.
- The year increments to cover for the 2009 technical plan are: 2009 (as a basis use the 2009 roadmap plus any known changes since then), 2011, 2013, 2015.

Test 5 year plan

Drivers
- Limited board test access
- Cost reductions
- Process optimization
- Test time reduction
- Outsourcing
- Environmental Requirements
- Time to Market

2007

Attributes

Min Test Pad Size (mils) - 20
Via / Pad Size (mils) – 24/10
BGA pitch – .4mm /.7mm
LF Substrate Materials
LF Board Finishes
Board node count – <15k
New LF solder alloys –
I/O Signal speeds – 10Ghz
High Density Interconnect (HDI)
Fault Coverage
Evolving fault spectrum
Bonding and Underfill of BGAs

Deployed Technology

Repeatable LF processes
Bead Probe
Adv. ICT
Adv. Boundary Scan & BIST

Research /Development

Bead Probe
Board Flex impact due to Pb-Free
Board Flex standard
Design for Test
Fault Coverage Metrology

2009

Attributes

Min Test Pad Size (mils) - 20
Probeable Micro Via / Pad Size (mils) – 11/5 (HDI)
BGA pitch – .4mm /.6mm
LF Substrate Materials
LF Board Finishes
Nodes – >15k
New LF solder alloys –
I/O Signal speeds > 20 Ghz
High Density Interconnect
Evolving fault spectrum

Deployed Technology

Bead Probe
Adv. Test Solutions
Adv. Boundary Scan & BIST
Common Diagnostics Model
Adv. Functional Test Solutions
Fault Coverage Metrology

Research /Development

Bead Probe
Board Flex impact due to Pb-Free
Board Flex standard
Design for Test
Adv. Test Solutions (HDI)

2011

Attributes

Min Test Pad Size (mils) –18
Micro Via / Pad Size (mils) – 12/5 (HDI)
BGA pitch – .3mm /.5mm
LF Substrate Materials
LF Board Finishes
Nodes – >15K
New LF solder alloys -
I/O Signal speeds >30 Ghz
High Density Interconnect
Evolving fault spectrum

Deployed Technology

Adv. Test Solutions
Adv. Structural Test
Adv. BIST
Virtual Access
Common Diagnostics Model
Adv. Functional Test Solutions

Research /Development

Adv. Test Solutions
Design for Test
New test techniques

2013

Attributes

Min Test Pad Size (mils) - 18
Micro Via / Pad Size (mils) – 12/5 HDI
BGA pitch – .3mm /.5mm
LF Substrate Materials
LF Board Finishes
Nodes – >15K
New LF solder alloys -
I/O Signal speeds >100 Ghz
High Density Interconnect
Evolving fault spectrum

Deployed Technology

Adv. Test Solutions
Adv. Structural Test
Adv. BIST
Virtual Access
Common Diagnostics Model
Adv. Functional Test Solutions

Research /Development

Adv. Test Solutions
Design for Test
New test techniques

Gap Analysis Charts

- The year increments to cover for the 2009 gap analysis charts are also: 2009 (as a basis use the 2009 roadmap plus any known changes since then), 2011, 2013, 2015.
- The GAP analysis chart (red, yellow, and green bar charts) is a forecast of technology status in the absence of iNEMI efforts. (Example follows for previous cycle)
- iNEMI projects should concentrate on the red and yellow areas where iNEMI effort is needed to develop the technology and/or bring it in earlier.
- This is the heart of the technical plan. The use of visuals (bar charts, time lines, color codes) convey a quick reference for the targeted audience.

Test Gap Analysis

2007 2009 2011 2013

Board

- Decreased Test Access-----------------------------
- Board Flex Standards-------------------------------
- Lack of Coverage Assessment Methods---------
- High speed signals (interposers) -----------------
- Lack of test solutions for HDI ----------------------
- Design for Test --
- Lack of Boundary Scan on digital devices ------

Functional, System

- Lack of Coverage Assessment Metrology-------
- At speed testing --------------------------------------
- Fault diagnostics-------------------------------------
- Lack of DFT standards (BIST) --------------------

Test equipment/Tools/Capabilities

- Node count exceeds tester capability-------------
- Need low cost test equipment---------------------
- Lack of test expertise at CMs/ODMs-------------
- New test solutions/strategies----------------------

Green = No Gap Issues or Resolved

Yellow = Known Gap Mitigation Techniques Red = No Known Solution – Development Required

What has changed

- What changes have occurred in recent years (2-3) that may have changed the content of the GAP Analysis and/or the 5-year plan (if one existed).
- New TIGs will need to describe changes (e.g. see Situation Analysis section in each chapter) highlighted in the 2009 technology roadmap. Highlight any critical items/showstoppers faced by the TIG.

TIG Plan

- In this section describe the projects and programs, from the Gaps and 5-year plan that the team will tackle in the next 1-2 years. Typically these projects are those that require deployment, implementation, and/or integration.
- Outline also what technologies require research to encourage either government agencies or universities to fund/pursue. Typically these require significant additional development and/or research, and may not be in iNEMI's scope.

Summary

- This is a good section to summarize key findings and final thoughts.

Format and Changes for the 2009 Technical Plan

- The plan will be bound in a booklet for easy distribution. Also to be made as an Acrobat document.
- MS Word will be used. Two columns per page for all the text parts. Embedded graphics for the charts.
- Each TIG's input will be a section within a chapter in the plan. The plan will include other brief introductory material about iNEMI, the roadmap, and the product sectors to give it completeness.
- The Research priorities will be published as a separate document again this cycle.
- The audience for this technical plan besides iNEMI members will be potential members, therefore the sections need to be self contained.
- Includes names of the latest TIG membership and contributors to each section (available from Secretariat)

2007 iNEMI Technical Plan Example

Microsoft Office
rd 97 - 2003 Docum

iNEMI

2007 iNEMI Research Priorities Example

Adobe Acrobat Document

Board Assembly TIG

Ian Williams, Intel

Advancing manufacturing technology

Organic Packaging Substrate TIG

Hamid Azimi, Intel

Advancing manufacturing technology

Board & Systems Mfg. Test TIG

Rosa Reinosa, HP
James J. Grealish, Intel

Advancing manufacturing technology

Organic PCB TIG

John Davignon, Intel

Advancing manufacturing technology

Medical TIG

Anthony Primavera, MSEI

Advancing manufacturing technology

Environmentally Conscious Electronics TIG

Scott O'Connell, Dell

Advancing manufacturing technology

Optoelectronics TIG

Brian Roche, Cisco
Tatiana Berdinskikh, Celestica

Advancing manufacturing technology