



INEMI[®]

International Electronics Manufacturing Initiative

2009 Technical Plan - Organic Substrate

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T.C. / TIG Meeting
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Advancing manufacturing technology

Technical Plan

- **Agenda**
 - **Introduction**
 - **Preliminary Five-year plan**
 - **What has changed**
 - **Preliminary Gap Chart**
 - **Preliminary TIG Plan**
 - **Projects/programs to focus on short term**
 - **Identify areas where research is needed**
 - **Summary**
 - **Back ups**

Organic Package Substrates

- **The Interconnect Organic Substrates Package**
TIG's primary objectives are to provide affordable substrate materials, processes, and equipment for products identified by the iNEMI Product Sectors and to benchmark current and to identify novel materials and manufacturing processes for enabling cost effective and reliable HDI substrates for high frequency packaging solutions encompassing 2-40 GHz.

Organic Package Substrate TIG 5 year plan

Drivers

-High Speed, High density Interconnect
-High frequency materials, HF, LF Materials

- Joint Reliability
-Process Integration

<p><u>Attributes</u> FF: 25x25 to 45x45 mm Thickness: 0.8-1.5 mm Layer #: 4-12 Line/Space: 15/15 Microvia size: 60-70um PTH/Pad: 200/350 SLI Pitch: 0.6 – 1.27 mm</p>	<p><u>Attributes</u> FF: 20x20 to 60x60 mm Thickness: 0.8 -1.8 mm Layer #: 4-12 Line/Space: 15/15 – 14/14 Micro via size: 60-70um PTH/Pad: 250/400 SLI Pitch: 0.4 – 1.27 mm</p>	<p><u>Attributes</u> FF: 20x20 to 60x60 mm Thickness: 0.8 -1.8 mm Layer #: 4-12 Line/Space: 14/14 – 12/12 Microvia size: 60-70um PTH/Pad: 250/400 SLI Pitch: 0.4-1.27mm</p>	<p><u>Attributes</u> FF: 15x15 to 60x60 mm Thickness: 0.6 -1.6 mm Layer #: 4-12 Line/Space: 12/12 – 10/10 Microvia size: 60-70um PTH/Pad: 200/375 SLI Pitch: 0.3-1.00 mm</p>	<p><u>Attributes</u> FF: 12x12 to 60x60 mm Thickness: 0.4-1.6 mm Layer #: 2-14 Line/Space: 10/10 – 8/8 Microvia size: 50-60um PTH/Pad: 180/350 SLI Pitch: 0.2-1.00 mm</p>
<p><u>Deployed Technology</u> Lead Free Solder Fine Line technology Tight alignment technology Thinner Core Smaller C4/BGA pitch</p>	<p><u>Deployed Technology</u> Lead Free Solder HF Materials Non-Contact testing Fine Line technology Smaller microvia technology Embedded Passives</p>	<p><u>Deployed Technology</u> Lead Free Solder HF Materials Fine Line technology Embedded passives Tight registration/patterning</p>	<p><u>Deployed Technology</u> Lead Free Solder HF Materials Fine Line technology Embedded passives Tight registration/patterning On Package voltage regulators</p>	<p><u>Deployed Technology</u> Fine Line technology Smaller microvias (Laser drill technology) Tighter registration/patterning Integrated actives/passives</p>
<p><u>Research and Development</u> Waveguide materials Mat'l Dimensional stability HF Materials High Frequency Materials Embedded passives/actives Non-contact testing Improved Warpage C4 bumping technology</p>	<p><u>Research and Development</u> On Package Voltage Regulators High Frequency Materials Waveguide Mat'l's FLS/ Registration Improved Warpage Patterning/registration Mat'l Dimensional stability</p>	<p><u>Research and Development</u> On Package Voltage Regulators High Frequency Materials Optoelectronic Mat'l's FLS/ Registration Improved Warpage Patterning/registration Mat'l Dimensional stability</p>	<p><u>Research and Development</u> High Frequency Materials Optoelectronic Mat'l's FLS/ Registration Improved Warpage Patterning/registration Mat'l Dimensional stability</p>	<p><u>Research and Development</u> Low CTE/High Tg HF material sets High Frequency Materials Smaller microvias Alternatives to conventional Fine L/S patterning Reduced pitch SLI joint reliability Non-solder based C4/Board contact</p>

2007

2009

2011

2013



What has changed

- The convergence of computer, entertainment media, and internet access is happening fast !
 - driving the need for more complex substrate
 - Example: reduced interconnect pitch → co-planarity, land size/alignment issues, solder mask, surface finish, and electrical test challenges.
 - Design for fabrication, assembly, test, cost, and quality & reliability.
 - Reliability based on use conditions
 - Example: With chip level power increasing and pitch decreasing, flip chip electro migration reliability decreases. Different redistribution methods and "embedded"/build up technologies need to be developed.
 - More complex supply chain mgmt / strategy !
 - Example: Streamlining multiple tiers of suppliers
 - Significant integration challenges in assembly and test technologies with smaller dimensional targets!
 - Example: Integrating thin substrate with thin silicon is a big challenge
 - Environmental regulations (Green requirements)
 - Cost Pressure !

What has changed

- Substrate no longer just a space transformer! It is becoming more like a circuit !
 - Higher performance systems , high density applications, RF, wire less, increase in bus speed, and broadband network usage are all driving substrate and packaging technologies for:
 - Integral inductive, resistive, and capacitive layers / embedded passives
 - higher electrical speed capability including tighter impedance control, better signal integrity and better thermal mgmt
 - smaller L/S, better via-to-pad and pad-to-via alignment, smaller uVias, smaller 1st and 2nd level pitch capability
 - Interconnect complexity
 - Optoelectronics
 - SiPs

What has changed

- BFR free is here! Mainstream starting in 2008 - 2010.
 - Removing Br usually reduces the Tg → wrong direction for lead free requirements → New mtl's and mt'l optimization needed!
 - Material processing and dimensional stability for BFR free mtls set currently pose a substantial manufacturing risk to the substrate industry.
 - Need wide range of materials (core, fluxes etc.) that meet reliability requirements.
- Surface finishes getting lots of attention, particularly for Lead Free
 - Immersion silver is gaining some additional users, but many OEM's have continued concerns – Ag migration/HAST risks.
 - Immersion Tin → restricted shelf life, planarity
 - Ni-Pd-Au, DIG, and direct solder on Cu are beginning to intercept and / or in late stage development.
 - For HDI substrates where power is an issue, barrier layer (Ni for example) is a MUST – hence many of PCB solutions are not applicable to HDI substrates!

What has changed

- System integration on packages is becoming essential.
 - Multi-chips/packages integration on a single substrate push for increased signal density
- Substrate dimensional requirements for form factor pushing at both sides of the spectrum
 - Handheld and ultra mobile PCs need small packages with higher functionality
 - integration of HDI manufacturing w/ LDI processing capabilities
 - Gaming and High-end PC's are becoming household commodity
 - Larger substrates (up to 70 X 70 mm at ≤ 0.5 mm pitch) w/ more complex features
 - 2nd level interconnect reliability
 - Substrate flatness requirement

What has changed

- Wide spread adoption of embedded capacitance
 - Expect wide adoption of embedded passives for network, SiP, and portable products
 - Improved design tools and material properties are needed for widespread adoption of embedded passives.
- Optoelectronic substrates are not yet making an impact as previously thought. All OEM's have said that they will use copper for their next generation machines; but work on mats have started.

Organic Substrate Gap Analysis

2007

2009

2011

2013

2015

Materials

	2007	2009	2011	2013	2015
Core materials/laminats					
Dimensional Stability	Green	Green	Yellow	Yellow	Red
Warpage	Green	Green	Yellow	Yellow	Red
High Tg, Low Dk, Low CTE, HF	Green	Green	Yellow	Yellow	Red
Buildup materials					
Low CTE/Low Profile materials	Green	Green	Yellow	Yellow	Red
Low Dimensional Variation	Green	Green	Yellow	Yellow	Red
Solder Mask materials					
Low Dimensional Variation	Green	Green	Yellow	Yellow	Red
Resolution/photoimageability	Green	Green	Yellow	Yellow	Red
Processes					
PTH/mechanical drilling	Green	Green	Yellow	Yellow	Red
Laser via (size and reliability)	Green	Green	Yellow	Yellow	Red
Via filling	Green	Green	Yellow	Yellow	Yellow
Overall registration	Green	Green	Yellow	Yellow	Red
Laser via alignment	Green	Green	Yellow	Yellow	Red
Litho buildup alignment	Green	Green	Yellow	Yellow	Red
Solder mask registration	Green	Green	Yellow	Yellow	Red
Surface finish	Green	Green	Yellow	Yellow	Red
Solder bumping	Green	Green	Yellow	Yellow	Red
Fine Line and Space	Green	Green	Yellow	Yellow	Red
Plating/trace dimensional control					
Reliability, trace deminsional and roughness variation	Green	Green	Yellow	Yellow	Red
Embedded discretes	Yellow	Yellow	Yellow	Yellow	Red

Green = No Gap Issues or Resolved

Yellow = Known Gap Mitigation Techniques Red = No Known Solution – Development Required



- **Tactical 1-2 yrs projects**
 - **Continue on surface finish project**
 - **Continue “manufacturability of BFR Free materials”**
 - **Add “standardization of reliability testing and evaluation of substrate/package reliability for emerging markets”**
 - **Netbooks and smart phones**

Organic Substrate Plan

- Technologies requiring significant R&D effort (>5 years – anybody in industry can work on it)
 - **Add HDI Substrate Standardization (attempt to standardize certain substrate process/material technologies)**
 - **Participants in iNEMI Organic Substrate package TIG should include substrate suppliers, equipment / material suppliers, customers of HDI substrates for an integrated effort at addressing current and future HDI Substrate related challenges.**

Summary

- Industry convergence of computing, communication and entertainment media with wireless applications has led to rapid growth in the use of HDI substrate technologies
 - The HDI Substrate manufacturing process is becoming more like a semiconductor fabrication process.
 - Opportunity for industry standardization on key metrologies, equipment and panel size?
 - Design for fabrication, assembly, test, cost, and quality & reliability is required as complexity and performance requirements increase, yet costs must remain stable.
 - Low cost fine line technology is at an inflection point for substrates, and new solutions and architectures are needed.
 - Integration challenges between substrate, assembly and test increasing
 - Thin substrate/ thin silicon integration is a big challenge !
 - Environmental regulations, reliability requirements, cost are adding additional challenges
- Participants in iNEMI Organic Substrate package TIG should include substrate suppliers, equipment / material suppliers, customers of HDI substrates for an integrated effort at addressing current and future HDI Substrate related challenges.

- 1. Surface Finish: With wider spread adoption of lead free solder on both chip and board sides, surface finish reliability to provide good solder joint connection, prevent non wet and discoloration issues which lead to yield losses and reliability risks**
- 2. BFR free technology widespread adoption is approaching. Need high focus on development of BFR Free materials that meet future substrate reliability challenges including thermal resistance, high Tg and low CTE**
- 3. Standardization of reliability testing and evaluation of substrate/package reliability for emerging markets**
- 4. HDI Substrate Standardization (attempt to standardize certain substrate process/material technologies)**

Initial Gaps for Organic Substrate

Medium Priority

- 5. Material development: Build-up dielectric and solder resist material developments to meet overall substrate design rule reliability requirements for IO densification and shrinking of plated features. In addition, any future requirements for fine line and space technologies should be compatible with materials selected for substrates.**
- 6. Embedded discrete: Resistor and capacitor embedding into substrate to shorten electrical return path between actives and board are needed to meet future power delivery requirements. This requires both material and process development to meet reliability and yield standards.**

Initial Gaps for Organic Substrate

Low Priority

- 7. Resolution and alignment targets: As patterns and features shrink in substrates more focus would be needed at developing processes and equipments to meet future alignment requirements. This entails more advanced laser and lithographic machines and potentially the move to overall photo-definable materials in place of laser to litho processes.**