iNEMI
International Electronics Manufacturing Initiative

2009 Technical Plan

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T.C. / TIG Meeting
Las Vegas, Nevada
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Advancing manufacturing technology

Technical Plan

- **Agenda**
  - **Introduction**
  - **What has changed**
  - **Preliminary Gap Chart**
  - **Preliminary Five-year plan**
  - **Preliminary TIG Plan**
    - **Projects/programs to focus on short term -prioritize**
    - **Identify areas where research is needed -prioritize**
  - **Summary**
  - **Back ups**

Introduction

- **This is the first year that the Organic Substrate TIG has been divided into two sections, the original Organic Substrate TIG and a new Organic PCB TIG**
- **The focus of this TIG is on Organic Printed Circuit Boards. (A decision on what market sectors or levels of technology will be encompassed or included in this TIG will be made in the future)**
- **The TIG has held two teleconferences with various industry leaders to define a preliminary gap assessment**

PCB Organic Substrate WG

- To improve the effectiveness of implementing cost effective bare PCB innovation and improve the quality and performance of electronic products in a global manufacturing environment
- Scope includes advancements in PCB design attributes, materials, electrical performance, reliability and process improvement for boards

What has changed

Status of PCB Industry/Concerns

- The breakout of Organic PCB from Organic Packaging Substrates was needed. The Package Substrate and PCB are integrally linked and dependent on each other progress.
- How do we parse such a large industry? By Product Sector Emulators?
- The move to an ODM Model is moving the PCB development/driver away from the OEM.
- New membership/participation makeup will need to include ODMs, PCB Fabricators, Laminate Suppliers
- PCB Suppliers have only a two year vision at best, not long enough to make revolutionary changes, hardly enough for evolutionary changes
- New product technologies demand more from supplier capabilities and are blurring the traditional market segmentation

Status of PCB Industry/Concerns, continued

- Many new processing and design challenges (e.g. increasing clock/data speeds, tighter impedance tolerances, PTH via to via distance barrier, registration, thermal management) Who pays for improvements?
- Continuous material changes (e.g. halogen free) due to RoHS present a challenge in cost, reliability, capacity, performance and metrology
- Product technology/design needs to drive Organic PCB innovation. (Are the Roadmaps where we are going or where we could go or where we would like to go?)
- Globalization of material and manufacturing process continues.
- Global consortiums have built in communication and integration difficulties (Time Zone/Face to Face meetings)

Preliminary GAP Analysis

"Organic PCB TIG"/Gaps/Technology Needs Summary -			
Priority	**< 5 Years (Tactical) Gaps/Needs**	**Category**	**Comments:**
	Process/Manufacturing		
	Dimensional consistency/stability. Materials viewpoint, low CTE, CTE mismatch, Thermal mismatch, Humidity control.		
	Improved dimensional stability materials (< 5yr)		
	Layer alignment accuracy		
	Finer line and space development		
	Improved drilling for less roughness and less runout (O)		
	Liquid crystal polymer that can be introduced into a PCB shop manufacturing process		
	Microvia technology improvement		
	Microvia metallization		
	Conformal Vs wide hole technology for reliability (uvia formation)		
	Surface Finishes		Bring back HASL, less problems than the new ones
	Boards without surface finishes		
	Reduced the land size of drill hole, Total Pad Stack improvement		
	Electrical Test		
	Electrical test: Embedded components/ Pitch & Pad size/ single testing cycle/ look at Test Gap Slide for areas of concern.		Test embedded components (actives & passives) prior to embedding and small pitch
	New non-contact testing techniques and new cost effective electrical test methods		
	Impedance testing and signal integrity		Bare board testing of crosstalk, loss and impedance at high speeds. More signal integrity analysis (VNA)
	High Speed Integrity/Designs		
	Process aspects		SI sensitive designs, more problems arising, How do you properly spec and measure impedance for high frequency. Signal Integrity gaps and upgraded HSIO
	Reliability		
	Reliability of smaller features, stacked uvia, composites		What about reliability of stacked uvias, composites, mechanics of
	Industry standard relibility testing		What about DnP and other mechanical testing to base to reliability
	Environmental concerns,		Concerns are what else in on the horizon, HF is being looked at now, what is next
	Embedded conponents,		Embedding actives in the board turns the board into a component how do you handle the reliability (ESD etc)
	Pad Cratering thermo machanical		HF showing more Thermo Mechanical rel problems
	Materials		
	High-performance & Halogen Free laminates that are competitively priced , Low Loss /Low Dielectric Constant are issues		High Speed and HF may not go hand in hand
	Integral materials for resistors / capacitors / inductors		

Preliminary GAP Analysis

"Organic PCB TIG"/Gaps/Technology Needs Summary -			
Priority	**< 5 Years (Tactical) Gaps/Needs**	**Category**	**Comments:**
	Design/Design Tools		
H	Two-way communication between designers/engineers and manufacturing personnel.		Large gap in communication between all levels of the manufacturing. What about design for manufacturing (DFx systems). How about building a Protocol System that notifies of changes and updates the schematics.
	Frequency barriers, high frequency concerns with materials, design, test? GHz		
	Improved design tools for emerging technologies like embedded passives and optoelectronic PCB's		Mentor said they were doing some design featues for optoelectronic. Design tools are driven by schematics
	Thermal Management, RF, Heat sink, high performance ASIC		How to manage the heat generated by these
	Embedded Passives		Based on a design stand point and toleranced by designers. Similar tolerances applied to embedded as though they were discretes.
	System board compression		integrating several boards into one board, using flex connection? Using HDI to move them into one boards, SIP architecture, Modular idea.
	Designer do not understand the effects of vias and pins fields and wonder why they get jitter. Far east designer may not be up to speed with the new speed requirements.Combination of both equipment and methodologies,		The design tools are too old for this or the designers do not want to learn to deal with these new speeds. CID course is 20 yrs old and does not address the newer speeds and designs. This is not being address because there is no dollars to upgrade this.
	Specifications		
	Gold thicknesses		Are the spec's real or even being followed, Dimm slots and cables, what is the reason for the thin gold, what is the reliability impact on the products
	Business/Economics		
	Understanding the true cost/performance relationship.		No cost vs. performance measurements for Printed Circuit designs. Layout efficiency? Only use cost per inch square. This is a poor metric, we need to get some better ones to answer this question. Cost Density analysis is one possibility
H	OEM to ODM move. How does that effect the system, R&D		
	Continuous cycle time reduction for quick turn boards.		Is this only a cost issue it ?
	Flexible circuit quick turn facilities		What is the basis for this concern?
	Time to Market		
Priority	**> 5 Years (Strategic) Gaps/Needs**	**Category**	**Comments:**
	Self reinforced materials	M	
	Alternate patterning processes (laser engraving for 8 um T/S, imprinting technologies)	Mfg	
	Non solder based interconnects	M	Very fruitful area, removing thermal parts of assembly would be good.
	Waveguide materials and manufacturing techniques	Mfg	Optical not cost effective, (not a RF waveguide concern?)

PCB 5 year plan

Drivers - increase signal speed - Cost reductions - Process optimization - pitch reduction/density increase - Outsourcing - Environmental Requirements - Time to Market

5 Year Plan Delayed until gap Analysis Completed

2009

Attributes
- Min Test Pad Size (mils) - 20
- Via / Pad Size (mils) – 24/10?
- BGA pitch – .4mm /.7mm
- LF Substrate Materials
- LF Board Finishes
- New LF solder alloys -
- Faster Signal speeds
- High Density Interconnect (HDI)

Deployed Technology
- Repeatable LF processes
- Bead Probe
- Adv. ICT
- Adv. Boundary
- Bonding

Research /Development
- Bead Probe
- Board Flex impact due to Pb-Free
- Board Flex standard
- Design for Test
- Fault Coverage Metrology

2011

Attributes
- Min Test Pad Size (mils) - 20
- Via / Pad Size (mils) – 24/10?
- BGA pitch – .4mm /.6mm
- HF Substrate Materials
- HF Board Finishes
- Nodes – >10k
- New LF solder alloys -
- Faster Signal speeds
- High Density Interconne
- Evolving fault spe

Deployed Technology
- olutions
- dv. Boundary Scan & BIST
- Common Diagnostics Model

Research /Development
- Bead Probe
- Board Flex impact due to Pb-Free
- Board Flex standard
- Design for Test
- Fault Coverage Metrology

2013

Attributes
- Min Test Pad Size (mils) - 18
- Via / Pad Size (mils) – ??
- BGA pitch – .3mm /.5mm
- LF Substrate Mate
- LF Board Fi
- Node
- s -
- speeds
- ensity Interconnect
- Evolving fault spectrum

Deployed Technology
- Adv. Test Solutions
- Adv. Structural Test
- Adv. BIST
- Virtual Access
- Common Diagnostics Model

Research /Development
- Adv. Test Solutions
- Design for Test
- New test techniques

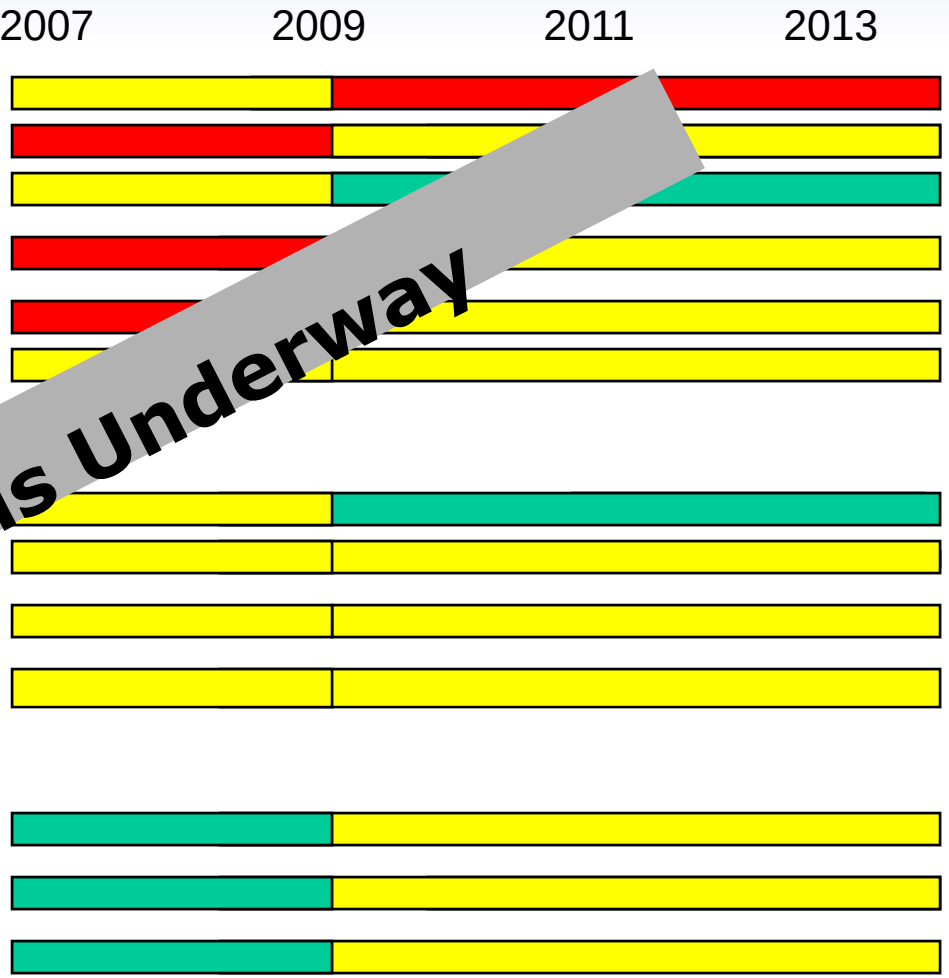
2015

Attributes
- is) - 18
- (mils) – ??
- – .3mm /.5mm
- Substrate Materials
- LF Board Finishes
- Nodes – >10K
- New LF solder alloys -
- Faster Signal speeds
- High Density Interconnect
- Evolving fault spectrum

Deployed Technology
- Adv. Test Solutions
- Adv. Structural Test
- Adv. BIST
- Virtual Access
- Common Diagnostics Model

Research /Development
- Adv. Test Solutions
- Design for Test
- New test techniques

Organic PCB Gap Analysis



Board

- Lack of Test Access----------
- Board Flex Standards----------
- Lack of Test Coverage Methods----------
- High speed signals----------
- Lack of test solutions for HDI ----------
- Design for Test ----------

Functional, System

- Lack of Test Coverage Methods ----
- High speed signals ----------
- Fault diagnostics----------
- Design for Test----------

Test eq ools/Capabilities

- Node cou xceeds tester capability ----------
- Need low cost test equipment----------
- Lack of supplier test expertise----------

Green = No Gap Issues or Resolved

Yellow = Known Gap Mitigation Techniques Red = No Known Solution – Development Required

Test Plan

- **Tactical 1-2 yrs projects**
  - **Add "Functional Test Coverage Model"**
  - **Add "Drive adoption of boundary scan ... as on digital components while ensuring industry is ready t... capability"**
- **Technologies r... ...g significant R&D effort (>5 years – an... ...y in industry can work on it)**
  - **Tes... ...d reliability performance of new lead free materials**
  - **Next generation DFT test techniques (e.g. beyond BIST and Boundary Scan)**

On hold until Gaps analyzed

Summary

- Presently pulling together the team to articulate the effects of the PCB gaps on the industry
- OEM to ODM outsourcing is changing the PCB industry interaction
- High Speed Signal Integrity will drive changes in test methods and the amount of testing required and when/what to test
- Thermal management needs to be understood,
- Designer education and design models/tools need upgrading for new technology levels
- Advanced HDI needs to have a focus on reliability not just manufacturing capability
- New materials need to be electrically and thermo mechanically sound not just environmentally sound

Back up Slide

Project Example: Reduced Via Footprint Opportunity

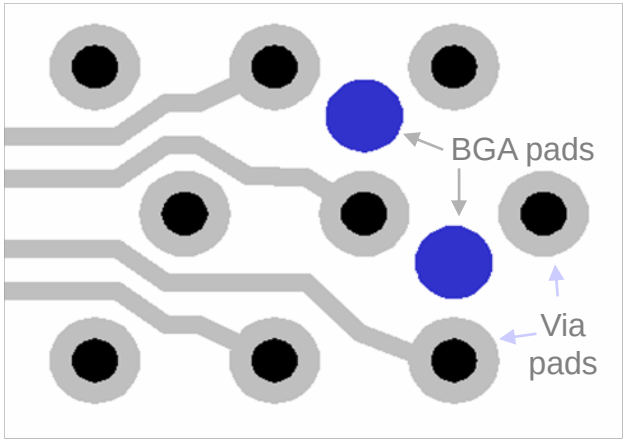
Via footprint currently limits BGA pad size and BGA pitch.

- Via footprint constitutes ~70% of pitch dimension for IO breakout
- Via footprint limits BGA pad size

Major PCB Contributors to Via Footprint:

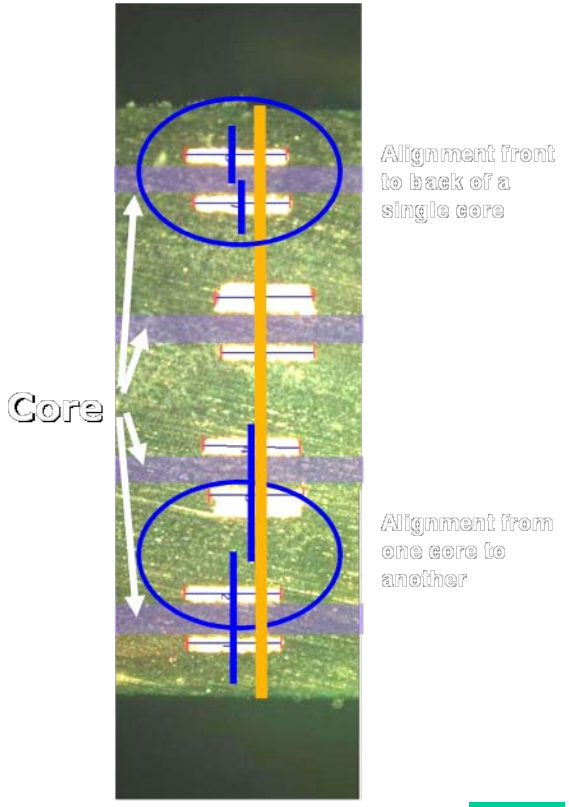
- Dimensionally stable or predictable material
- Alignment core to core and front to back of a single core
- Drill Registration
- Via size

Land Pattern



30% Trace/ Space

70% Via footprint



Future pitch reduction efforts should be focused on the largest contributor to the overall via footprint: Material, registration, and via size.