# 2009 Technical Plan- Board & System Test TIG

*TIG Chair*
*T.C. / TIG Meeting*
*Las Vegas, Nevada*
*April 3, 2009*

Advancing manufacturing technology

# Technical Plan

- **Agenda**
  - **Introduction**
  - **Tech Plan Update**

# Board & Systems Test TIG

- Chair: Rosa Reinosa (HP)
- Co-Chair: James Grealish (Intel)

# Test

- To improve the effectiveness of the test process and the quality of electronic products in a global manufacturing environment
- Scope includes test technology and process improvement for boards and systems (e.g. automated inspection, electrical test, boundary scan, functional test, system test)

# Gap Analysis Update (1 of 2)

1) Developed list of gaps (from current roadmap & participating companies)
2) Discussed each gap
3) Gathered inputs
4) Completed prioritization (11 companies voted)

# Gap Analysis Update (2 of 2)

- **Participating companies (12)**
  - Huawei (Victor Chen)
  - Cisco (Steve Butkovitch)
  - Dell (Phil Geiger)
  - Agilent (Ken Parker)
  - HP (Skip Meyers, Rosa Reinosa)
  - TRI (Floyd Conner)
  - Boston Scientific
  - Asset (David Bonnet)
  - Jabil (David Anthus)
  - Delphi (Mike Reagin)
  - Plexus (Tim Kruse)
  - Intel (James Grealish)

# Initial Gaps for Test

## Top Priority

1) What do we do when ICT fails to deliver the coverage needed based on current trends where lack of access is becoming a bigger challenge (i.e. hdi, high speed buses); a number of technologies came out to help out with some of these issues (i.e. bead probe, VTEP, IBIST).

# Initial Gaps for Test

## Medium Priority

2) Influence board layout tools with incorporated features to be capable of addressing testability issues. Vision for Design for Test and strategy tools interacting together. Is there a way that DFT tools can make use of strategy tools findings and apply it to the design. Incorporating knowledge of testability solutions at the time the board is being layout would be useful. Can speed up decisions upstream. If there is a test strategy known, how can we transfer it to the cad layout system so that it is addressed just in time to be incorporated early? Can end up with a more effective test and save money down the road.

3) Lack of Defect Coverage Tools (particularly for functional / systems test): Lack of tools that allow the defect coverage of a value stream to be documented and verified.
   - Difficult for an OEM to understand what coverage gaps exist in a value stream before an issue occurs.
   - Difficult to analyze redundancy / overlap in defect coverage in a value stream

# Initial Gaps for Test

## Medium Priority

4) Imaging technologies need improved capability and lower capital and operating costs to meet the challenges of increased defect rates associated with Lead Free and less effective ICT due to trends of continually reducing electrical access and increasing board complexity.
   - AOI - Needs a reduction in false fails and escape rates.
   - AXI – Needs cycle time improvements and reduction in false failures and escape rates.
   - Need to address what this means in the context of Agilent exiting this business. May become a major industry gap with new players and tools.
   - AXI systems need to keep pace with miniaturization.

5) It is difficult to determine the relationship between product faults and the defects which cause those faults. This is becoming more of an issue as product designs allow for less component level test coverage.
   - Given a functional test of a product, how may product defect coverage be determined?
   - If a fault exists, how may it be mapped back to the defect to facilitate repair?

# Initial Gaps for Test

## Medium Priority

6) As ICs have adopted lower supply voltages, the proliferation of low-voltage power requirements at elevated current levels has become a growing concern. Boards now convert higher-level voltages on-board, into a set of lower voltages at high currents. This on-board DC-DC converter circuitry tends to be difficult to test and can introduce new hazards such as thermal events and IC damage when regulated voltages are not achieved.

7) Lack of modeling/design tools to determine what level of BIST and testability support should be designed into a product?

8) Need current tools to be able to deal with component/packaging hierarchy issues to address testability (i.e. multi-core processors)?

9) Lack of modeling/design tools to be able to tell how much test is enough for a particular product

# Initial Gaps for Test

**Low Priority**

10) The lack of access has a partial solution with boundary-scan but it needs increased adoption in digital devices, and the use of the new 1149.6 specification for high-speed differential digital signals, to be truly successful

11) Lack of improvements in the cost and capability of TIM fixturing and tooling

12) Lack of modeling/design tools to be able to tell where a particular TIM Technology should be placed in a product's process flow

# Next Steps

- Complete Test Gap Analysis
- Discuss project opportunities for FY10
- Complete Project Plan

# Back-up Slides

# Test 5 year plan

**Drivers**

- Limited board test access
- Cost reductions
- Process optimization
- Test time reduction
- Outsourcing
- Environmental Requirements
- Time to Market

## 2007

**Attributes**

Min Test Pad Size (mils) - 20
Via / Pad Size (mils) – 24/10?
BGA pitch – .4mm /.7mm
LF Substrate Materials
LF Board Finishes
Board node count – <10k
New LF solder alloys -
Faster Signal speeds
High Density Interconnect (HDI)
Fault Coverage
Evolving fault spectrum

**Deployed Technology**

Repeatable LF processes
Bead Probe
Adv. ICT
Adv. Boundary Scan & BIST
Bonding and underfill of BGAs

**Research /Development**

Bead Probe
Board Flex impact due to Pb-Free
Board Flex standard
Design for Test
Fault Coverage Metrology

## 2009

**Attributes**

Min Test Pad Size (mils) - 20
Via / Pad Size (mils) – 24/10?
BGA pitch – .4mm /.6mm
LF Substrate Materials
LF Board Finishes
Nodes – >10k
New LF solder alloys -
Faster Signal speeds
High Density Interconnect
Evolving fault spectrum

**Deployed Technology**

Bead Probe
Adv. Test Solutions
Adv. Boundary Scan & BIST
Common Diagnostics Model

**Research /Development**

Bead Probe
Board Flex impact due to Pb-Free
Board Flex standard
Design for Test
Fault Coverage Metrology

## 2011

**Attributes**

Min Test Pad Size (mils) - 18
Via / Pad Size (mils) – ??
BGA pitch – .3mm /.5mm
LF Substrate Materials
LF Board Finishes
Nodes – >10K
New LF solder alloys -
Faster Signal speeds
High Density Interconnect
Evolving fault spectrum

**Deployed Technology**

Adv. Test Solutions
Adv. Structural Test
Adv. BIST
Virtual Access
Common Diagnostics Model

**Research /Development**

Adv. Test Solutions
Design for Test
New test techniques

## 2013

**Attributes**

Min Test Pad Size (mils) - 18
Via / Pad Size (mils) – ??
BGA pitch – .3mm /.5mm
LF Substrate Materials
LF Board Finishes
Nodes – >10K
New LF solder alloys -
Faster Signal speeds
High Density Interconnect
Evolving fault spectrum

**Deployed Technology**

Adv. Test Solutions
Adv. Structural Test
Adv. BIST
Virtual Access
Common Diagnostics Model

**Research /Development**

Adv. Test Solutions
Design for Test
New test techniques

## What has changed

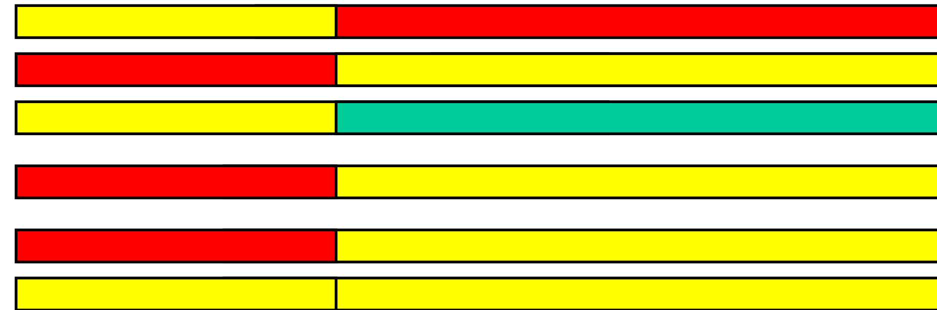
- Need a cost effective manufacturing test process that addresses evolving product technology needs
- Many new test challenges (e.g. increasing clock and data speeds, smaller test targets, limited test access on PCAs, lead free impact, more complex devices, underfill/edge bonding of BGAs)
- New product technologies demand more from supplier capabilities
- Globalization of test and manufacturing process
- Continuous material changes (e.g. halogen free, flux, paste, new solder alloys) due to RoHS present a challenge
- Test equipment, tools and fixturing need to follow product technology
- Complex devices require DFT (BIST and Boundary Scan) features to improve board and system test coverage

# Test Gap Analysis

2007 2009 2011 2013

## Board

- Lack of Test Access-----------------------------------
- Board Flex Standards--------------------------------
- Lack of Test Coverage Methods------------------
- High speed signals----------------------------------
- Lack of test solutions for HDI -----------------------
- Design for Test -----------------------------------------



## Functional, System

- Lack of Test Coverage Methods ------------------
- High speed signals ----------------------------------
- Fault diagnostics----------------------------------------
- Design for Test----------------------------------------

## Test equipment/Tools/Capabilities

- Node count exceeds tester capability -----------
- Need low cost test equipment----------------------
- Lack of supplier test expertise---------------------

Green = No Gap Issues or Resolved

Yellow = Known Gap Mitigation Techniques Red = No Known Solution – Development Required

# Test Plan

- **Tactical 1-2 yrs projects**
  - Add “Functional Test Coverage Model”
  - Add “Drive adoption of boundary scan standards on digital components while ensuring industry is ready to leverage capability”

- **Technologies requiring significant R&D effort (>5 years – anybody in industry can work on it)**
  - Testability and reliability performance of new lead free materials
  - Next generation DFT test techniques (e.g. beyond BIST and Boundary Scan)

# Summary

- Limited test access on Printed Circuit Assemblies will drive significant test technology changes in industry
- Use of common test metrics can help drive the quality of electronic products
- Cost pressures continue to drive changes in OEM test strategies
- Boundary scan initiatives must be linked to other industry work (e.g. IEEE Bscan Standards)
- Globalization of the test process requires..
  - New ways of managing product quality
  - Improved supplier capabilities in Asia Pacific