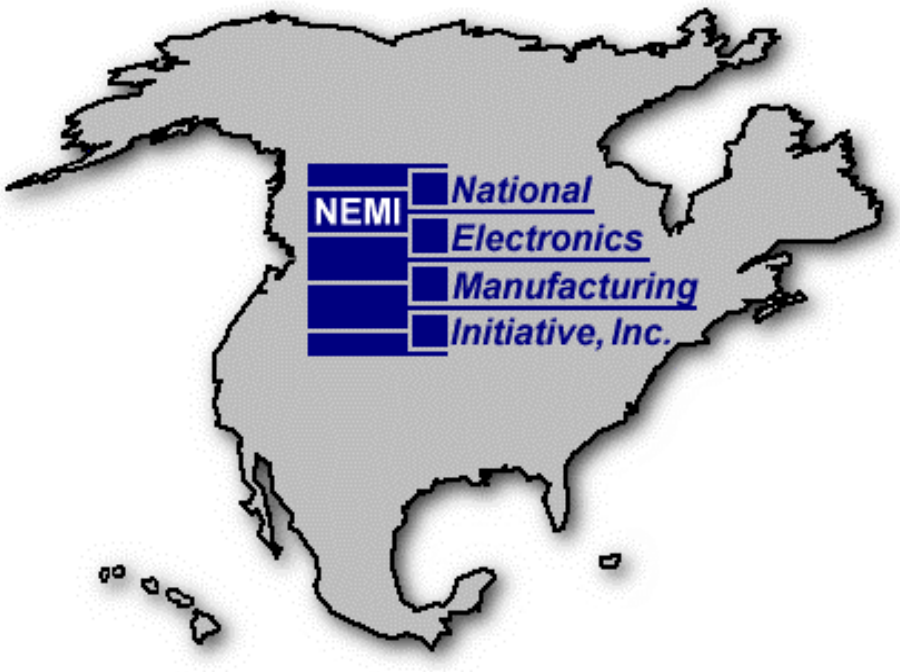


Lead Free Reliability Team Status

John Sohn

Lucent Technologies - Bell Labs

Reliability Team Leader

January 17, 2001

Agenda

- Acknowledgements
- Statement of Work
- Reliability Tests
- Component-Paste Combinations
- Test Matrix
  - Components
  - Boards
- Thermal Cycling
  - Data Analysis
  - Failure Analysis
- Other Tests
- Schedule

Acknowledgements
NEMI Lead Free Reliability Team (Active)

Rick Arnold	Motorola	Carol Handwerker	NIST
Jasbir Bath	Solectron	Brian Hunter	StorageTek
Elizabeth Benedetto	Compaq	Keith Johnson	Kodak
Dennis Bernier	Kester Solder	Kevin Knadle	IBM
Edwin Bradley	Motorola	Jim Kopec	FCI
Rick Charbonneau	StorageTek	Jack McCullen	Intel
Jana Cousineau	Alcatel	Rich Parker	Delphi Delco
Mike DiPietro	IEEC	Len Poch	Universal Instr
Ken Fallon	Kodak	Swami Prasad	ChipPac
Charlie Fieselman	Solectron	Svetlana Reznik	Kodak
Al Gickler	Johnson Mfg	Marianne Romansky	Celestica
Ron Gedney	NEMI	Tom Siewert	NIST
David Godlewski	NEMI	John Sohn	Lucent
Frank Grano	SCI	Adam Zbrzezny	Celestica

Statement of Work - Reliability

Main Task: Perform reliability testing for selected solders, components and board finishes using an approved test vehicle

- Define the test requirements
- Determine environmental withstanding levels
- Design and fabricate test vehicles
- Perform reliability tests; carry out failure analysis and determine root cause
- Document results

Additional Activity: Promote modeling for reliability

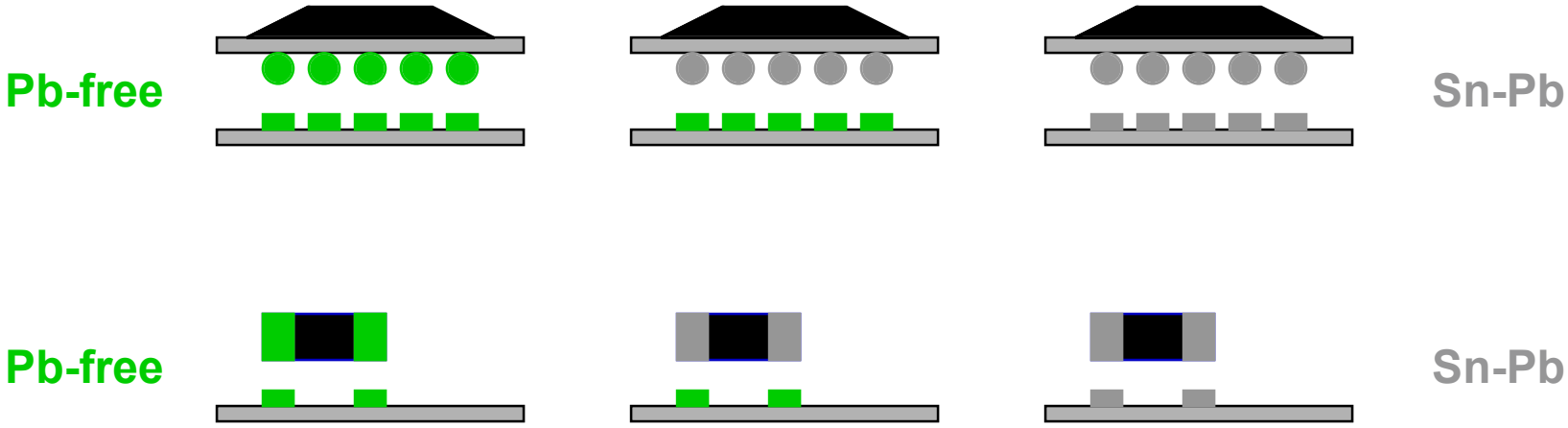
Reliability Testing

- **Thermal Cycling**
  - 2 temperature regimens
  - 32 components per test cell
  - 9 full cells, 1 partial cell
  - 6 test locations
- **Electrochemical Migration**
  - solder paste evaluation
- **Bend Testing**

Component-Paste Combinations

Three component/paste combinations

Paste: Sn3.9Ag0.7Cu, Sn3.0Ag0.5Cu, and Sn37Pb
Component terminations: Pb-free and SnPb

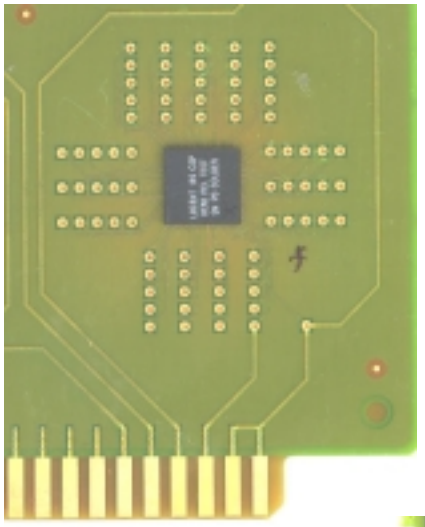


Test Matrix

Component	Source	Description	Reliability Testing	
			-40 to 125°C	0 to 100°C
Type 1 TSOP	AMD	48 Pin TSOP with leads on short sides, SnPb and NiPd finishes	Solectron	
2512 Resistor		zero ohm chip resistor, SnPb and pure Sn finishes	SCI	
169 CSP	Lucent	0.8mm pitch, 11x11mm, 7.7mm^2 die, SnAgCu and SnPb balls	Kodak	Lucent
208 CSP (HDPUG)	ChipPac	0.8mm pitch, 15x15mm, 8.1 mm^2 die, SnAgCu and SnPb balls	Kodak (both SnAgCu alloys)	SCI
256 BGA (NCMS)	Amkor	1.27mm pitch, 27x27 mm, 10 mm^2 die, SnAgCu and SnPb balls	Celestica	SCI
256 CBGA	IBM	1.27mm pitch, no die, SnAgCu and SnPb balls	Motorola	

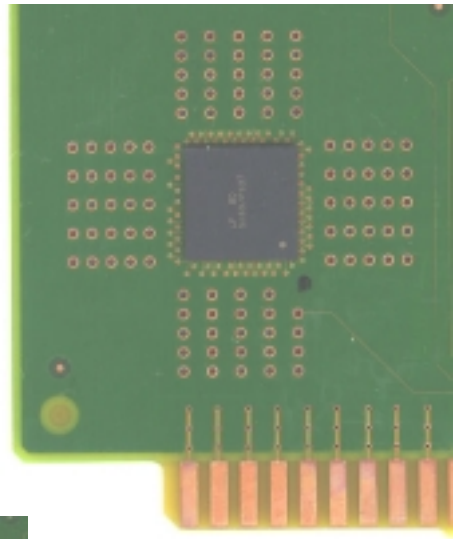
SnAgCu balls: Sn4.0Ag0.5Cu - provided by Hereaus

Assemblies: 4 area array packages per board



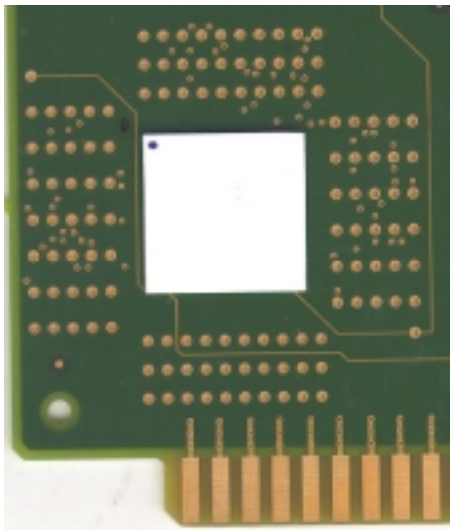
169CSP

256BGA

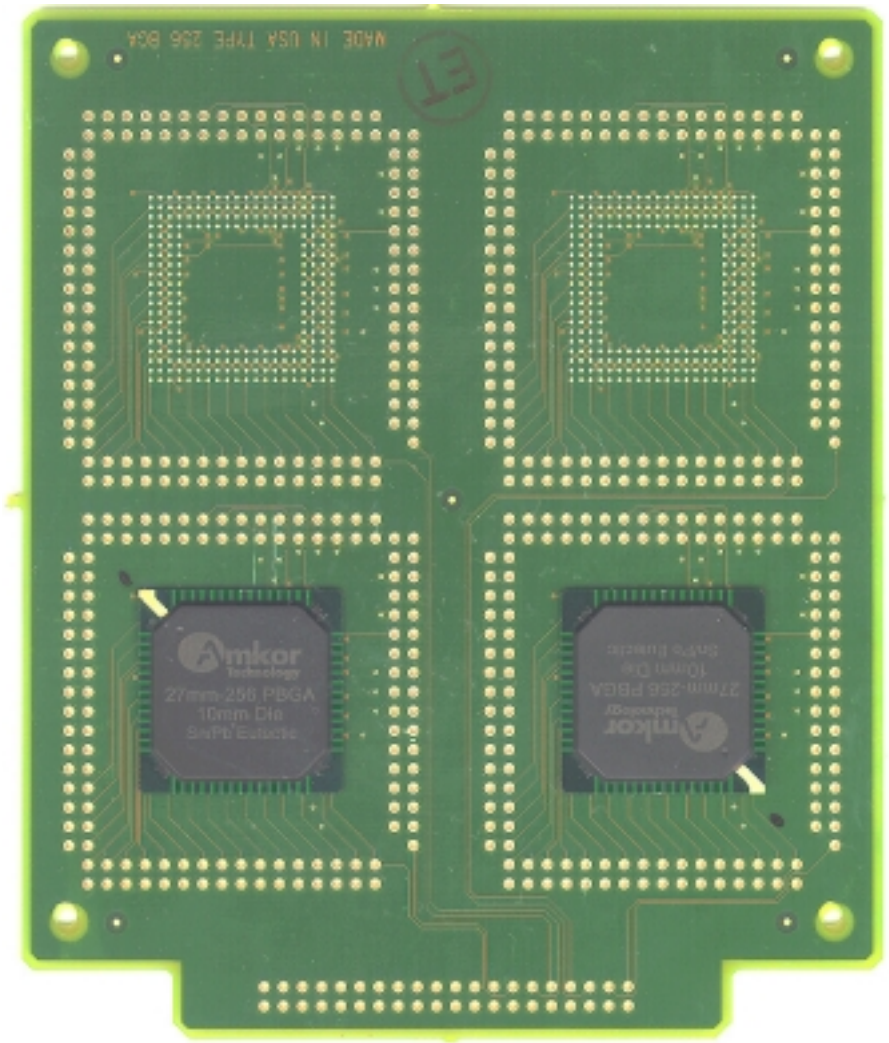


208CSP

256CBGA



256BGA Test Board



Thermal Cycling Conditions

Per JEDEC JESD22-A104B (July 2000) "Temperature Cycling", with additional requirements

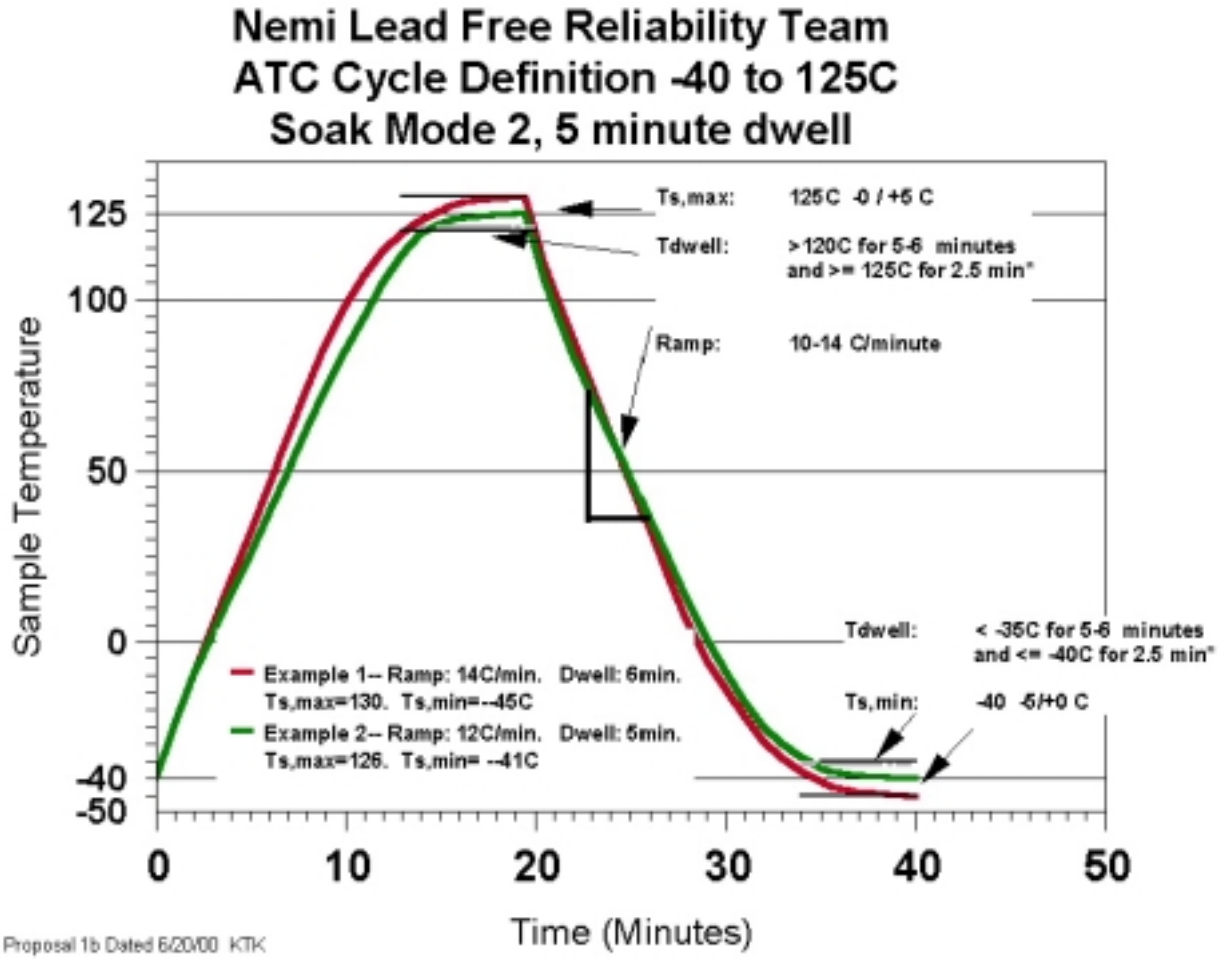
- -40 (+0,-5) to 125 (+5,-0) °C (Condition G of Table 1)
- 0 (+0,-5) to 100 (+5,-0)°C (Condition J of Table 1)

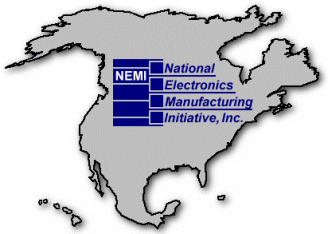
Ramp: 10-14 C/minute, calculated linearly between 10% and 90% of Delta-T range

Dwell : Soak mode 2 of Table 2 (5 minute minimum dwell) defined with "5-degree" dwell clock. Additional dwell criteria: At least 1/2 of the dwell time (2.5 minutes) must be at or beyond the target temperature.

Measurement: All specified temperatures are of the test samples, not the chamber air, and must be verified in situ on sufficient # of samples prior to start of test.

Thermal Cycling Profile (example)





Failure Criteria

Per IPC-SM-785 "Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments"

Failure detection shall be by continuous monitoring of daisy-chain continuity test loops such that:

1. At least one continuity interruption of one microsecond or less duration can be recorded for each test loop during any polling interval of two seconds or less;
2. At least 10 such interruptions can be recorded per test loop to confirm the first failure indication;
3. The monitoring current does not exceed 2mA at no more than 10V and that an electrical discontinuity is indicated by a loop resistance of 1000 ohms or more. False failure indications due to electrical noise can be a problem, particularly for loop resistance thresholds lower than 1000 ohm.

Data Formatting and Analysis

JMP Discovery statistical software package (Version4.0.2) by SAS Institute.

Information

- stress test conditions
- component type
- component-paste combination
- board, component ID
- cycles and censoring (comp failure, test complete, etc)
- cause of failure
- initial and final resistance values (4 pt measurement)

Failure Analysis

T_0 Information

- x-ray, C-SAM, AOI (post-assembly, pre-cycling)
- cross-section one component per each component type, check for intermetallics, stand-off height; use assembly retain
- Visual inspection (10-30x)

Post Cycling - failed parts and surviving parts

- Visual inspection (10-30x)
- C-SAM analysis
- Dye penetration, pull testing
- Cross section failed area(s) - failure modes, crack paths, intermetallics, voids, void sizes, joint height
- SEM analysis of intermetallics

Bend Testing, Electrochemical Migration

- **Bend Testing**

  3 point bend on PBGA component to simulate the damage that occurs from out of plane deformation during drop, test, or assembly.

  To be performed by Compaq

- **Electrochemical Migration (pastes)**

  Conditions: IPC-TM-650 Method 2.6.14.1, 65°C/85%RH/10V, 500h

  Test coupon: IPC B25A, Pattern D (12.5 mil lines/spaces)

  To be performed by paste suppliers

Schedule

- Thermal Cycling: February - May 2001
- Failure Analysis: May - June 2001
- Data Analysis: May - July 2001
- Bend Testing: February - March 2001
- Electrochemical Migration - complete July 2001
- Final Report: August 2001