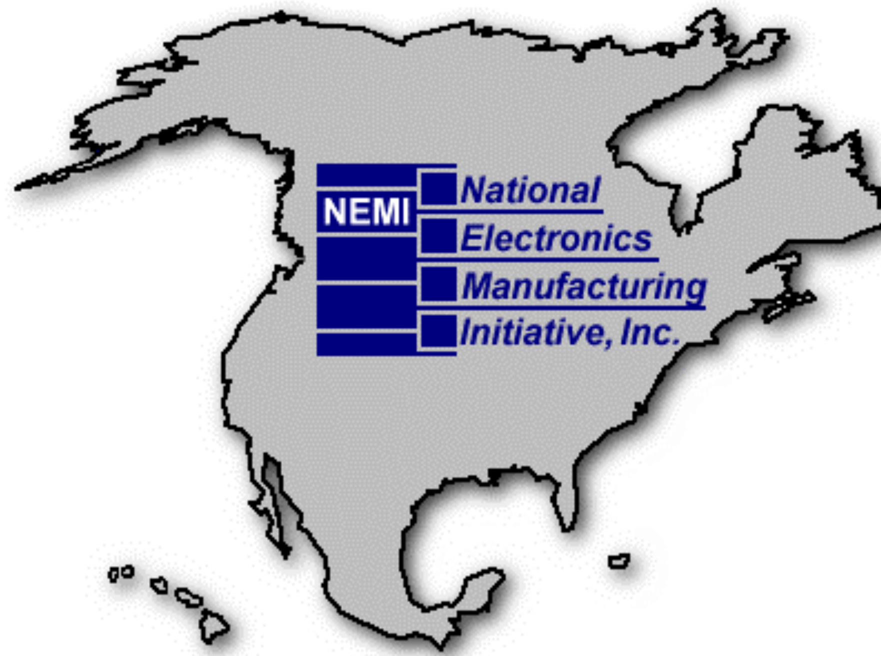
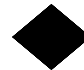


Lead Free Component Team Status

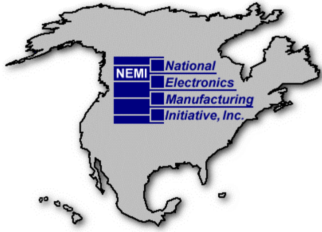


Richard Parker

Delphi Delco Electronics Systems

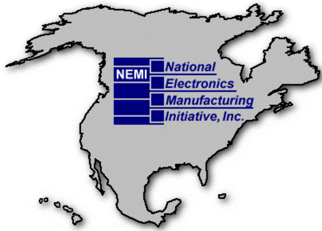
Component Team Leader

01-17-01



Agenda

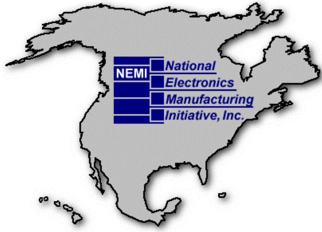
- Acknowledgements
- Requirements issues
  - Peak reflow temperatures
  - Profile pattern
  - Time to peak reflow temperature
- Impact on ICs (Case studies)
  - Summary of observations
- Moisture Sensitivity Level Study Conclusions
- Component Lead Finishes
- Component Labeling Concerns
- Summary of Accomplishments



Acknowledgements

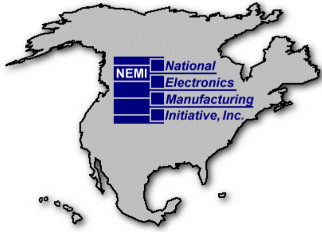
- **NEMI Lead Free Component Team (Active)**

Name	Company
Srinivas Chada	Motorola
Jim Kopec	FCI USA Electronics Corp
Ron Gedney	NEMI
Dave Godlewski	NEMI
Nick Lycoudes	Motorola
Jack McCullen	Intel
Sean McDermott	Celestica
Swaminath Prasad	ChipPAC
John Sohn	Lucent
Edgar Zuniga	Texas Instruments
Jack Fisher, et al.	ITRI
Richard Parker	Delphi Delco Electronics Systems



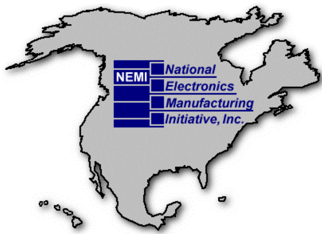
Requirements Issues: Peak Temperature

- Higher peak reflow temperatures (PRT)
  - Established 260 °C (-5/+0) °C joint temperature: Worst case for all components to be evaluated against
    - NEMI IC Users defined target temperature
      - Celestica, Delphi, Motorola, Solectron, CE, etc.
    - Japan customers (Sony, etc.)
- 260 °C was picked to accommodate the spectrum of small boards to large back-plane boards
- Solder joint wetting performance is a function of temperature
  - Hotter is better, so users tend to prefer hotter ♦ Larger process window
  - Managing thermal mass of circuit board & components is a processing issue. (Want low delta T.)



Requirements Issues: Peak Temperature (cont.)

- Measurement location of PRT creates issues depending on point of reference
  - Top center surface of the package (JEDEC & supplier reference point)
  - Lead / solder joint temperature (Users reference point)
- The user's goal is to balance cycle time (throughput) with peak temperature
  - Smaller temperature deltas require slower conveyor speeds
- The process goal is to reflow the solder at the joint with some margin of safety (process window)
  - Allowance must be made for the coldest part to solder
  - Small thermal mass parts may get much hotter



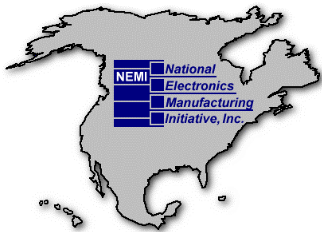
Example Thermal Profile of Large Board

14 ^{o}C Delta

235C
183C
163C
150C
105C
92C
20C

	C1 = 0+00:01:35	C2 = 0+00:03:10	C3 = 0+00:04:45	C4 = 0+00:06:20
U86 Center Solder Joint	104	154	196	173
C13 Pin 1 Solder Joint	106	153	195	167
U56 CBGA Body	114	155	204	154
Fab near J59	134	165	218	137
U79 Pin 7	108	156	198	163

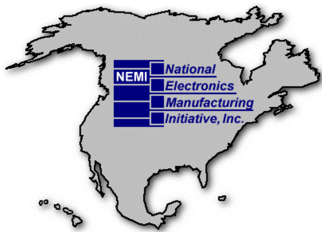
Connect with and Strengthen Your Supply Chain



Impact of Peak Reflow Temp. on MSL

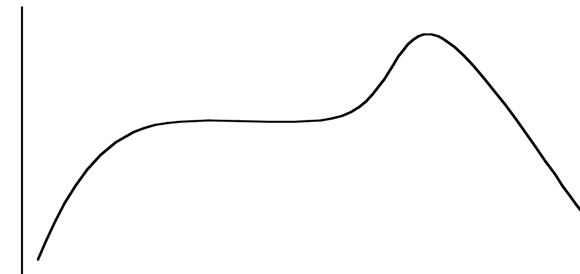
- **Moisture Sensitivity Level (MSL) rating is a primary concern for IC manufacturers and IC users alike**
  - **This rating determines humidity exposure limitations prior to using in a reflow soldering process**
  - **Level 1 is the best, level 6 is the worst (bake before use)**

MSL	Conditions	Floor Life	Dry Bake required	Dry Pack required
1	≤ 30 C/85%RH	Unlimited	no	no
2	≤ 30 C/60%RH	1 year	Optional	yes
2a	≤ 30 C/60%RH	4 weeks	yes	yes
3	≤ 30 C/60%RH	168 Hrs	yes	yes
4	≤ 30 C/60%RH	72 Hrs	yes	yes
5	≤ 30 C/60%RH	48 Hrs	yes	yes
6	≤ 30 C/60%RH	Mandatory Dry Bake before use. Reflowed within time specified on label.		yes



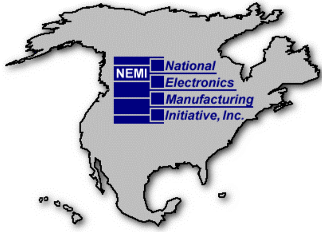
Requirements Issues

- **Profile with preheat hold**
  - **Used on larger & multilayer boards**
  - **Japan, Europe, NEMI users**



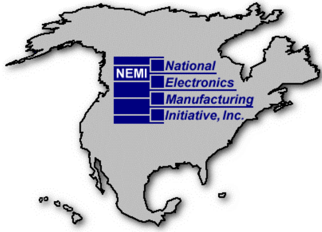
PROFILE ELEMENTS	CONVECTION
Ramp rate 50 °C to 150 °C	2 °C/sec min
Preheat temperature 180 °C	120 seconds max.
Average ramp-up rate 190 °C To225 °C	2.2 °C/sec min
Temperature maintained above 217 °C	60-150 seconds
Time within 5 °C of actual peak temperature	10-20 seconds
Peak temperature range	255 °C (+5/-0) °C
Ramp-down rate	6 °C /second max.
Time above 165 °C	3 - 5 minutes

- JEDEC Moisture Sensitivity Level (MSL) data is usually run with this type of profile
- Profile has an impact on MSL performance
- Peak temperature was varied for MSL testing (220-225, 235-240, 250-255, 255-260 °C)



MSL Data Analysis

- **4 Suppliers preformed Pb-free MSL analysis**
- **Case Studies were performed with:**
  - **SOICN (Narrow Body)**
  - **SOICW (Wide Body)**
  - **SOP**
  - **PLCC**
  - **QFP / LQFP / MQFP / PQFP / TQFP**
  - **PBGA / TBGA / uBGA**



Data for IC Packages

SOIC-N Package Vs. MSL Vs. Peak Reflow Temperature

MSL

6
5a
5
4
3
2a
2
1
0

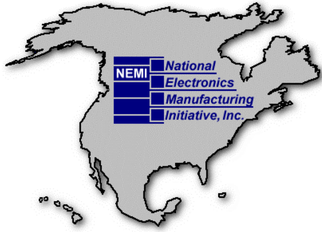
220 - 225 °C
235 - 240 °C
250 - 255 °C
255 - 260 °C

S1 S1 S2 S2 S3
S1 S1 S2 S2
S1 S1 S2 S2 S3
S1 S2

8 14 16 16

Lead count

S1, S2, S3, etc. = S1 is existing package structure; S2 is improved package structure; S3 is further improved package structure; S1, S2, S3 may not be the same for each package tested (i.e. new mold compound, assembly equipment, die coat, etc.)



Data for IC Packages

SOIC-W Package Vs. MSL Vs. Peak Reflow Temperature

220 - 225 °C
235 - 240 °C
250 - 255 °C
255 - 260 °C

MSL

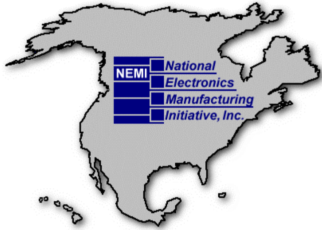
6
5a
5
4
3
2a
2
1
0

S1 S1 S2 S3
S1 S1 S2 S3
S1 S2
S1 S1 S2 S2 S3
S1 S1 S2 S2 S3

16 20 20 24 28

Lead count

S1, S2, S3, etc. = S1 is existing package structure; S2 is improved package structure; S3 is further improved package structure; S1, S2, S3 may not be the same for each package tested (i.e. new mold compound, assembly equipment, die coat, etc.)



Data for IC Packages

Package Vs. MSL Vs. Peak Reflow Temperature

MSL: 6, 5a, 5, 4, 3, 2a, 2, 1, 0

SOP | SSOP | TSSOP

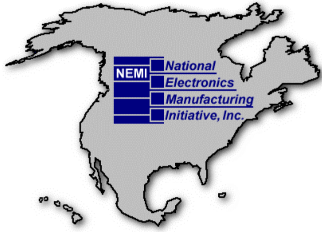
220 - 225 °C
235 - 240 °C
250 - 255 °C
255 - 260 °C

S1 S2 | S1 S2 | S1 S1 S2 | S1 S1 S2 | S1 S1 S2 | S1 S2 | S1 S2 | S1 S1 S2 | S1 S1 S2

24 | 20 | 38 | 56 | 20 | 28 | 32 | 56 | 64

Lead count

S1, S2, S3, etc. = S1 is existing package structure; S2 is improved package structure; S3 is further improved package structure; S1, S2, S3 may not be the same for each package tested (i.e. new mold compound, assembly equipment, die coat, etc.)



Data for IC Packages

Package Vs. MSL Vs. Peak Reflow Temperature

TVSOP Exposed Die Pad

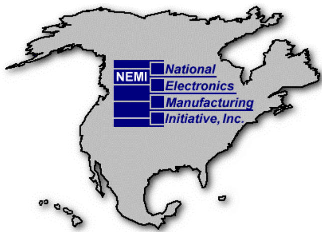
MSL: 0, 1, 2, 2a, 3, 4, 5, 5a, 6

Legend: 220 - 225 °C; 235 - 240 °C; 250 - 255 °C; 255 - 260 °C

Lead count	S1 (220 - 225 °C)	S1 (235 - 240 °C)	S2 (255 - 260 °C)
56 (TVSOP)	1	1	2
28 (Exposed Die Pad)	1		2
32 (Exposed Die Pad)	2		3
100 (Exposed Die Pad)	3		4

Lead count

S1, S2, S3, etc. = S1 is existing package structure; S2 is improved package structure; S3 is further improved package structure; S1, S2, S3 may not be the same for each package tested (i.e. new mold compound, assembly equipment, die coat, etc.)



Data for IC Packages

PLCC Package Vs. MSL Vs. Peak Reflow Temperature

MSL: 0, 1, 2, 2a, 3, 4, 5, 5a, 6

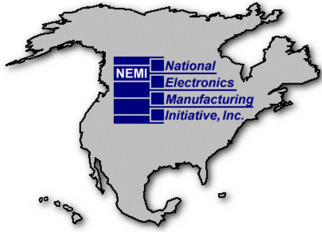
220 - 225 °C
235 - 240 °C
250 - 255 °C
255 - 260 °C

S1 S1 S2 S2 S3
S1 S1 S2 S2 S3
S1 S1 S1
S1 S1 S2 S3
S1 S1 S2 S3
S1 S1

28 44 44 52 68 68

Lead count

S1, S2, S3, etc. = S1 is existing package structure; S2 is improved package structure; S3 is further improved package structure; S1, S2, S3 may not be the same for each package tested (i.e. new mold compound, assembly equipment, die coat, etc.)



Data for IC Packages

QFP Package Vs. MSL Vs. Peak Reflow Temperature

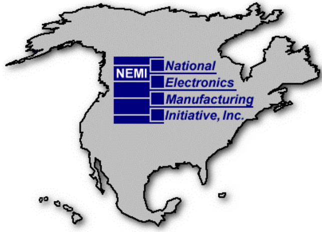
MSL: 0, 1, 2, 2a, 3, 4, 5, 5a, 6

Lead count: 44, 44, 48, 52, 64, 100, 128

Legend: 220 - 225 °C; 235 - 240 °C; 250 - 255 °C; 255 - 260 °C

Bar labels: S1 S2 S2 S3 | S1 S1 S1 | S1 S2 S2 S3 | S1 S2 S2 S3 | S1 S2 S2 S3 | S1 S2 | S1 S2

S1, S2, S3, etc. = S1 is existing package structure; S2 is improved package structure; S3 is further improved package structure; S1, S2, S3 may not be the same for each package tested (i.e. new mold compound, assembly equipment, die coat, etc.)



Data for IC Packages

Package Vs. MSL Vs. Peak Reflow Temperature

MSL

6
5a
5
4
3
2a
2
1
0

LQFP
MQFP
PQFP
TQFP

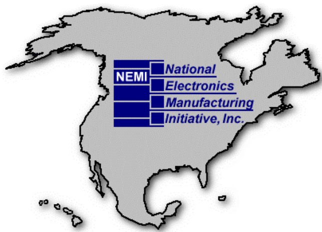
S1 S2

64 100 144 208 208 132 64 100 176

Lead count

220 - 225 °C
235 - 240 °C
250 - 255 °C
255 - 260 °C

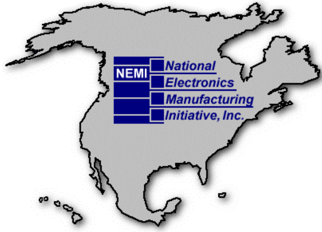
S1, S2, S3, etc. = S1 is existing package structure; S2 is improved package structure; S3 is further improved package structure; S1, S2, S3 may not be the same for each package tested (i.e. new mold compound, assembly equipment, die coat, etc.)



Data for IC Packages

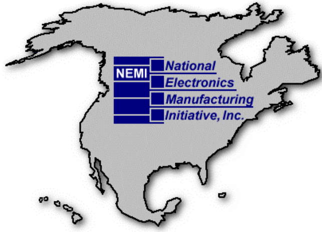
Package Vs. MSL Vs. Peak Reflow Temperature

S1, S2, S3, etc. = S1 is existing package structure; S2 is improved package structure; S3 is further improved package structure; S1, S2, S3 may not be the same for each package tested (i.e. new mold compound, assembly equipment, die coat, etc.)



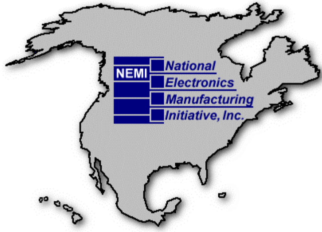
Summary of MSL Data

- Team thoroughly analyzed the MSL Data
  - There is no generic solution for maintaining an IC's MSL with a higher reflow profile
- Generally, smaller, thinner packages have better results, but
  - data is confounded by package construction
  - construction and materials employed have major impact
  - material & process interactions are not completely understood yet



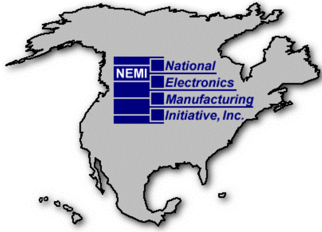
Summary of MSL Data (cont.)

- **All ICs must be reclassified for the Pb free applications and the impact to Moisture Sensitivity Level (MSL)**
  - **Factors affecting MSL {from JEDEC Specs.}**
    - **Die attach materials and processes**
    - **Number of pins**
    - **Mold compound material and process**
    - **Die pad area and shape**
    - **Body size**
    - **Passivations / die coating**
    - **Lead frame / heat spreader design materials and finish**
    - **Die size and thickness**
    - **Wafer fabrication process**
    - **Interconnect**
    - **Lead lock tape used in molding process**



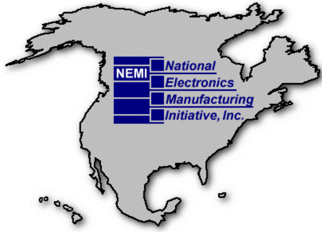
Summary of MSL Data (cont.)

- Moisture Sensitivity Level (MSL) Rating:
  - MSL typically degrades by one level for every 5 to 10 °C increase of PRT
  - Degradation of MSL may increase with increasing profile dwell above 200 °C
- Potential for substantial number of "Bake Before Use" parts
  - Newer package structures (materials, etc.) may reduce the MSL degradation but increase costs
  - More qualifications will be needed
    - Cycle time & cost impact
- Construction of the IC makes a difference in MSL



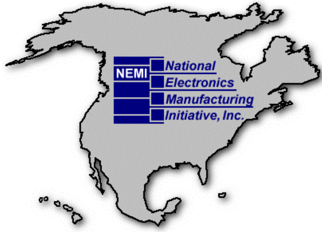
Conclusions from MSL Studies

- **Set the peak reflow temperature as low as possible.**
  - **Targeting joint temperatures 240 to 245 °C would be beneficial**
    - **Maintaining a minimal "delta T" across the circuit board will allow lower peak temperature profiles**
    - **The step from 225 to 240 °C will be a modest impact to the IC supplier**
    - **The step from 240 to 250 °C will be a bigger impact**
    - **The step from 250 to 260 °C is huge!**
  - **Newer convection cure ovens will perform better for larger circuit boards with high thermal mass components**
- **Is 260 °C really required?** *[Yes, for some users]*
  - **Is recycling large / complex circuit boards a better solution?** *[Yes, but that's a separate issue]*



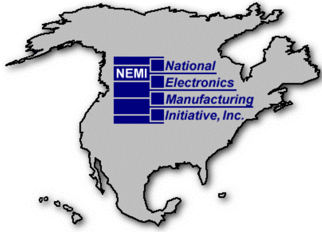
Component Surface Finishes

- Most Promising component lead finishes choices
  - NiPdAu, Sn, SnBi, SnCu
- Circuit board finish choices
  - OSP, Sn, Ag, Ni/Immersion Au
- Issues and concerns
  - Solder wetting
  - Cost (relative to incumbent finish)
  - Plating process complexities
  - Tin whiskering
- Need to maintain compatibility with existing SnPb solder alloys (i.e., no negative impacts to joint reliability)



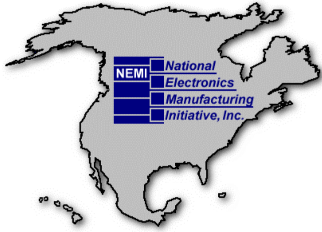
Component Labeling; Initial Look

- Identifying Pb-free components will be required by the most OEM users
  - Transition to lead free parts will be made on a product basis, driven by customers (timeframe is years)
    - Both lead free and the previous finish could be run on the same lines during the transition period
- Data sheets must clearly identify Pb-free status
  - Lead finish alloy composition should be defined
  - Reflow temperature limitations should be defined
- OEMs preferred solution is to change part number (or add suffix) to facilitate in house tracking
- Labeling options will be studied by IC suppliers & standards committees in the coming months



Accomplishments Summary

- 2Q99: conducted vendor survey
  - Majority of suppliers were unaware with no plans
- Developed and published a component reflow profile
- Engaged ITRI for help in assessing PWB finishes
- Engaged ITRI to determine effect on PWB laminates
- Obtained boards for reliability testing
- Second vendor survey underway
- MSL Study on plastic semiconductor packages
  - Working with 4 major suppliers to quantify component impacts
  - Have presented initial MSL data results at APEX 2001



Appendix “A”

Glossary of IC Terms

BGA	Ball Grid Array
JLCC	J-Leaded Ceramic or Metal Chip Carrier
LCCC	Leadless Ceramic Chip Carrier
LGA	Land Grid Array
LQFP	Low Profile Quad Flat Pack
PDIP	Plastic Dual-In-Line Package
PFM	Plastic Flange Mount Package
QFP	Quad Flat Package
SIP	Single-In-Line Package
SOJ	J-Leaded Small-Outline Package
SOP	Small-Outline Package (Japan)
SSOP	Shrink Small-Outline Package
TQFP	Thin Quad Flat Package
TSSOP	Thin Shrink Small-Outline Package
TVFLGA	Thin Very-Fine Land Grid Array
TVSOP	Thin Very Small-Outline Package
VQFP	Very Thin Quad Flat Package
LPCC*	Leadless Plastic Chip Carrier
MCM	Multi-Chip Module
MQFP	Metal Quad Flat Package
PLCC	Plastic Leaded Chip Carrier
PPGA	Plastic Pin Grid Array
SDIP	Shrink Dual-In-Line Package
SIMM	Single-In-Line Memory Module
SODIMM	Small Outline Dual-In-Line Memory Module
TSOP	Thin Small-Outline Package
VSOP	Very Small Outline Package