



inEMI

International Electronics Manufacturing Initiative

International Technology Roadmap for Semiconductors

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Design ITWG
SMTAI, Orlando, FL
10/12/07*

Advancing manufacturing technology



ITRS Roadmap Design + System Drivers ***The New Scaling of Silicon Systems***

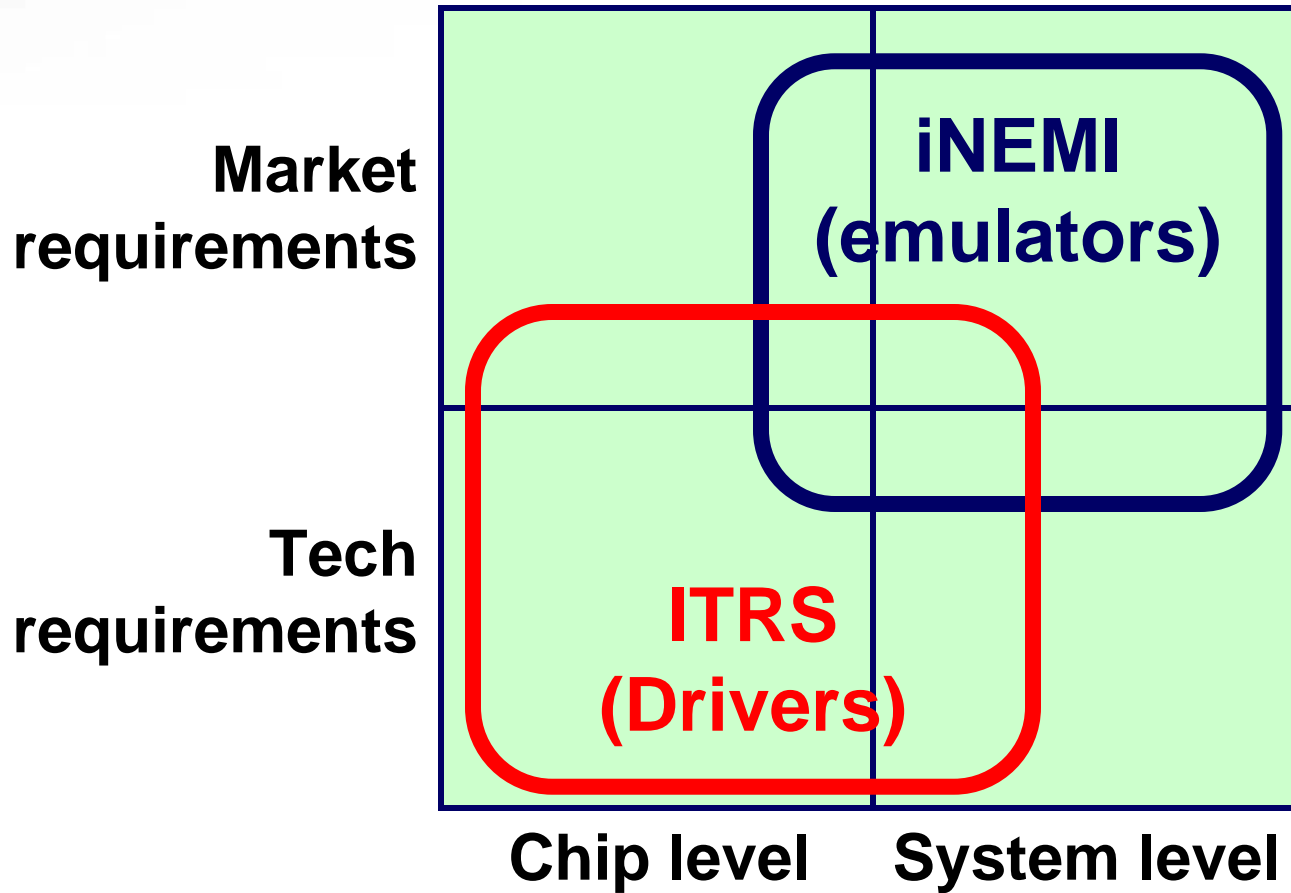
iNEMI October Meeting, Orlando

Worldwide Design TWG

Presented by Juan-Antonio Carballo



ITRS-iNEMI Domain Space



The Message

1. ITRS Design Group focuses on roadmapping:

1. **Design Chapter:** Technology challenges and solutions
2. **System Drivers Chapter:** Types of silicon systems

2. ITRS addressing new systems scaling

Conventional (Moore) + Heterogeneous (Moore+) scaling

3. ITRS being aligned by market/application driver

“Fabric” drivers – market independent

CPU, DSP/SPU, memory, AMS

With iNEMI!

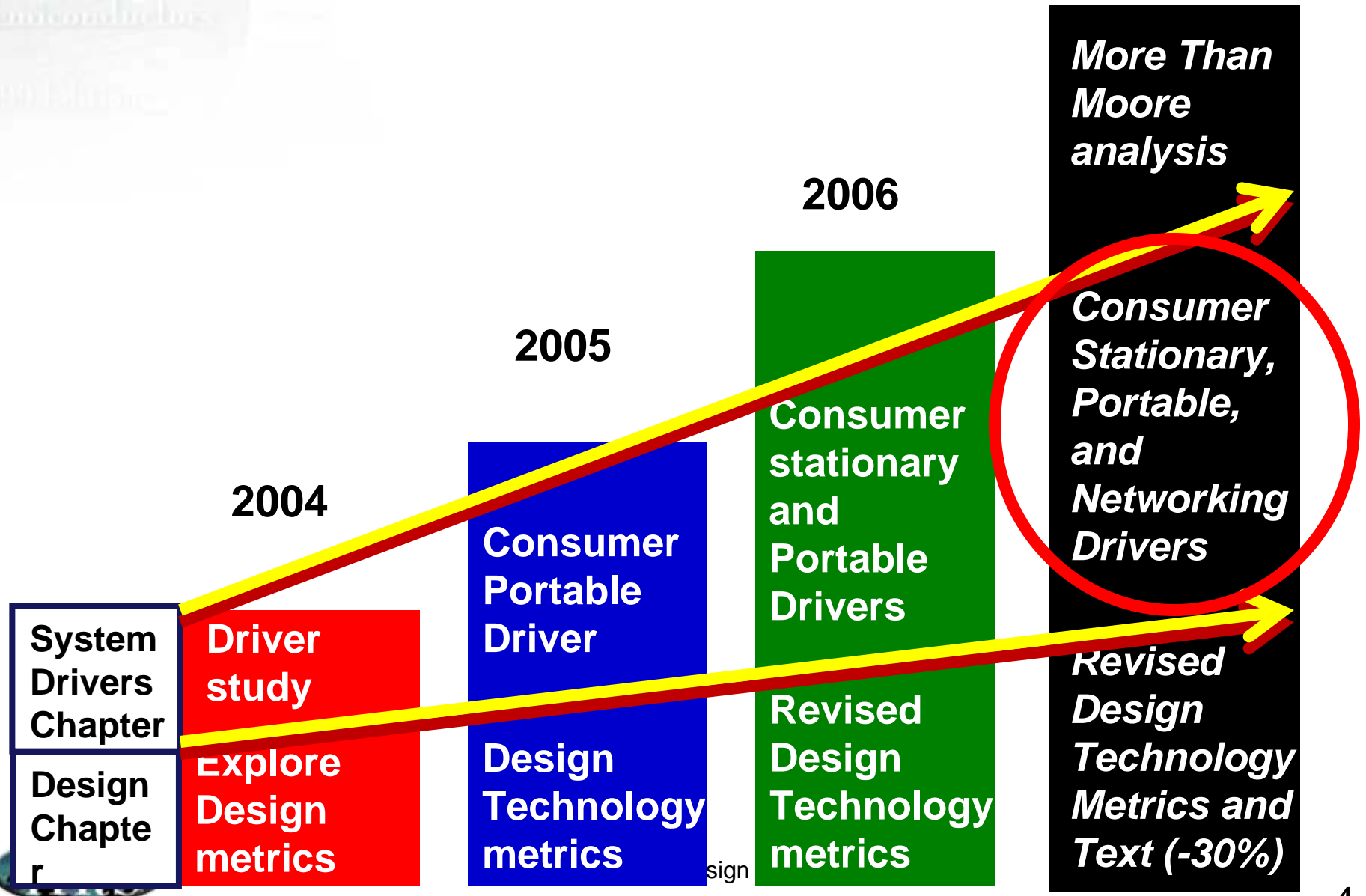
“Market” drivers – market dependent

consumer mobile and stationary, networking, office



ITRS Design + System Drivers

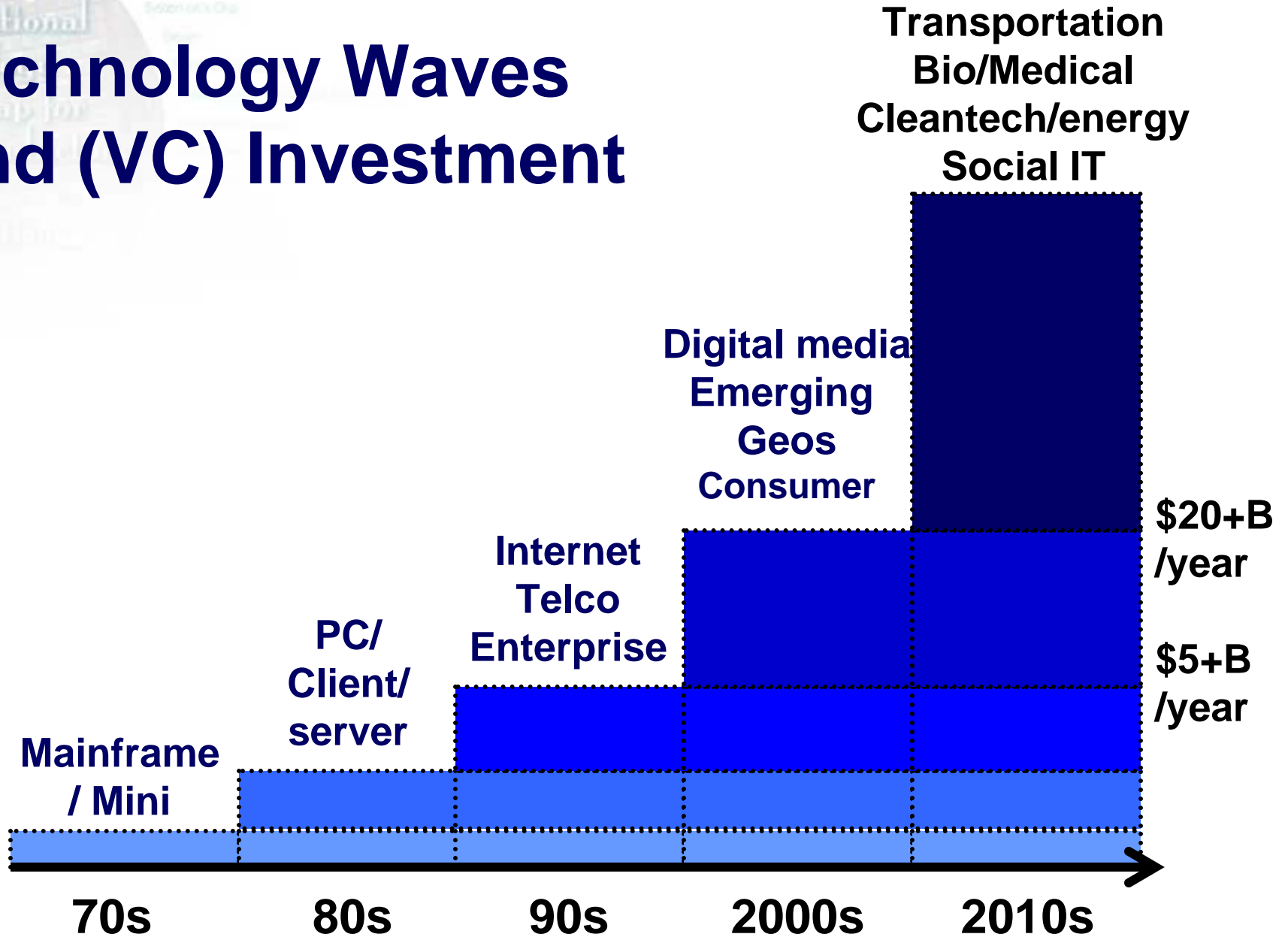
2007



The New Scaling of Silicon Systems

Different Market Drivers Scale Differently

Technology Waves And (VC) Investment



Source: insight from Top VCs including Walden
ITRS Design TWG 2007



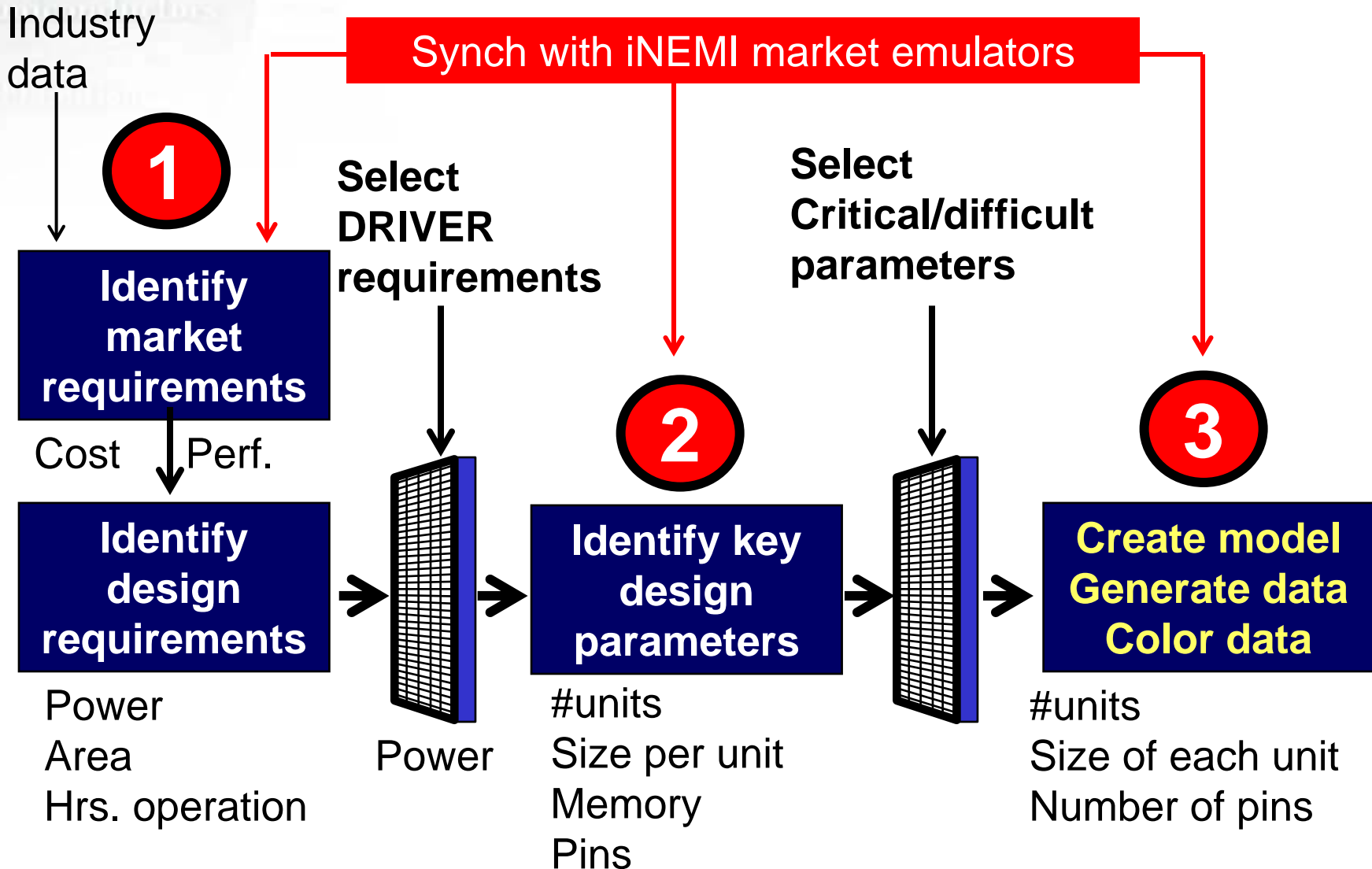
Driver Template

Driver parameter	Example	Units
Market requirements (customers AND suppliers)	Cost, Performance Energy consumption / battery life Time to market Reliability	\$ / unit Pages / sec Hours Months Years
Critical design requirements	Power, Area, Time per operation / clock speed Latency / throughput / bandwidth Design productivity Hours of operation	Watts mm ² GHz Nano-secs PY/ mm ² Hours
Critical design parameters	Memory size / bandwidth # processing units, redundant units Size and clock speed/BW of each unit Number of pins	Bytes <None> Mm ² <None>

System (Market) Drivers Evolution

Driver	Market ST/LT requirements	Design requirements	Design parameters	Leader
Office/PC (processor)	(General) Performance	Clock cycle MIPS, FLOPS	#of cores memory	US 2005
Consumer (portable)	Energy cost	W, hours of operation (energy)	# of cores, voltage, clock cycle, etc.	Asia 2005 (Japan)
Consumer (stationary)	(Media/emerg) performance	Frames/sec, FLOPS	# of SPUs, memory BW, etc., latency	Asia 2006 (Japan)
Network (comms.)	Bandwidth	G/Tbits/sec	# of I/Os, BW per I/O, etc.	US 2007
Automotive (industrial)	Reliability Accuracy	Years, max/min T, radiation, sensing accuracy	% redundancy	EU 2008
Medical	Heterogeneous Integration?	Analog, digital, chemical, bio, sensors, etc.	#of (bio, chem) sensors on-chip,	EU 2008
Defense	Reliability (extreme)	Years, max/min T, radiation,	Redundancy	USA 2009

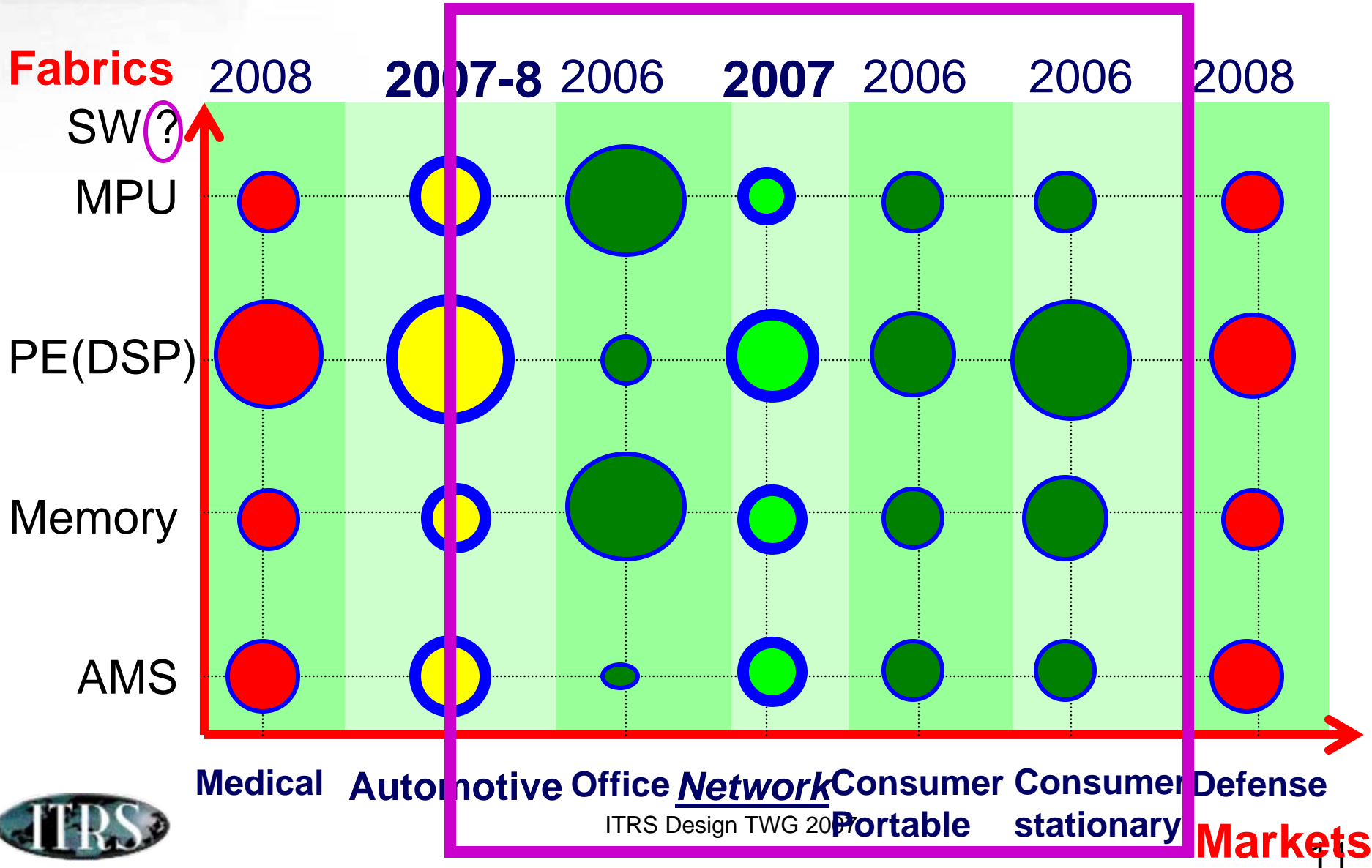
Process For Each System Driver



Template Plan For System Drivers

	ISSCC (USA) FEB	Spring (EU) APRIL	Summer (USA) JULY	ICCAD (USA) NOV	Winter (Asia) DEC
Process	Agree				
Market and design reqs and parameters	Discuss line items	Agree on line items			
Tables		Have some data	Have all data		Plan next year
Text			Have some text	Text finished, link to chapters	

An Expanded Set of Drivers Will Direct An Increasingly Broad Industry



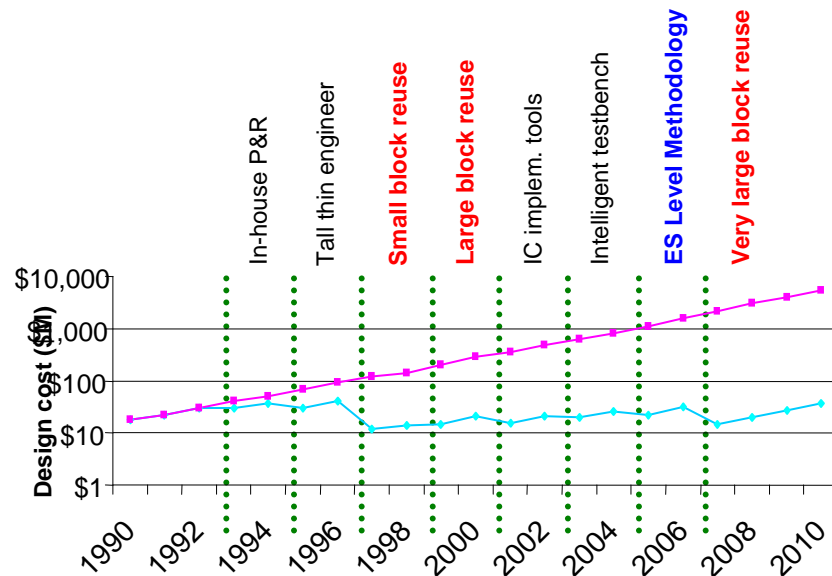
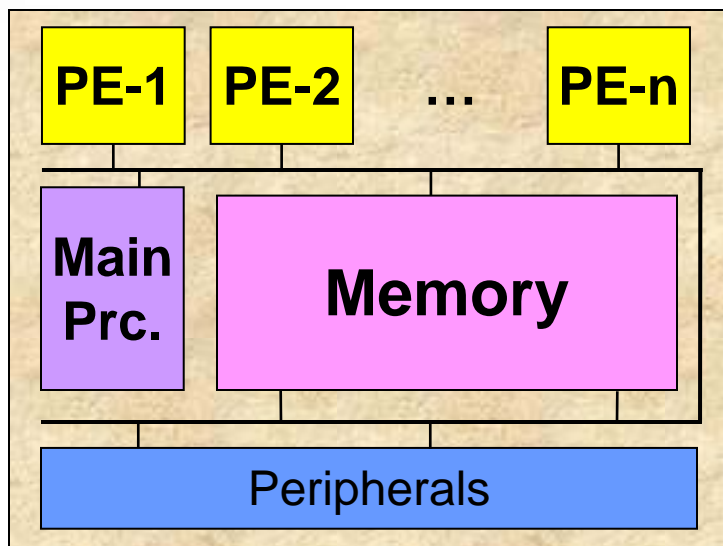
The New Scaling of Silicon Systems

Consumer Market Driver -- Portable

Consumer Portable System Driver

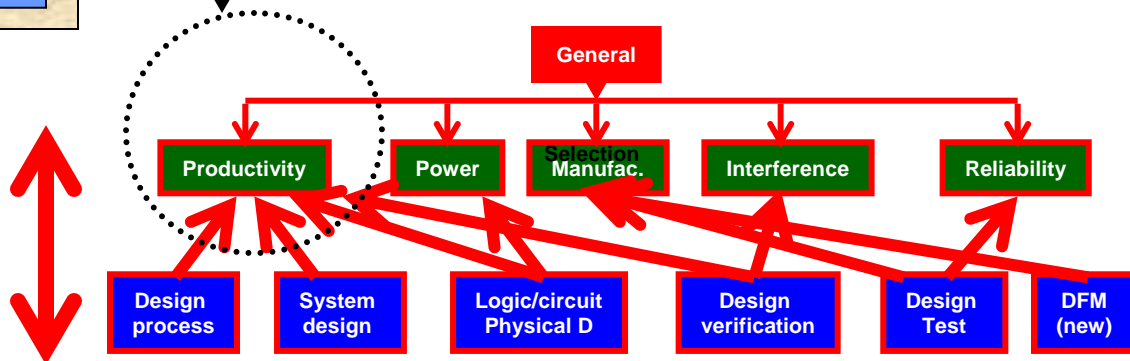
(Japan Design TWG)

Mobile /Consumer SoC

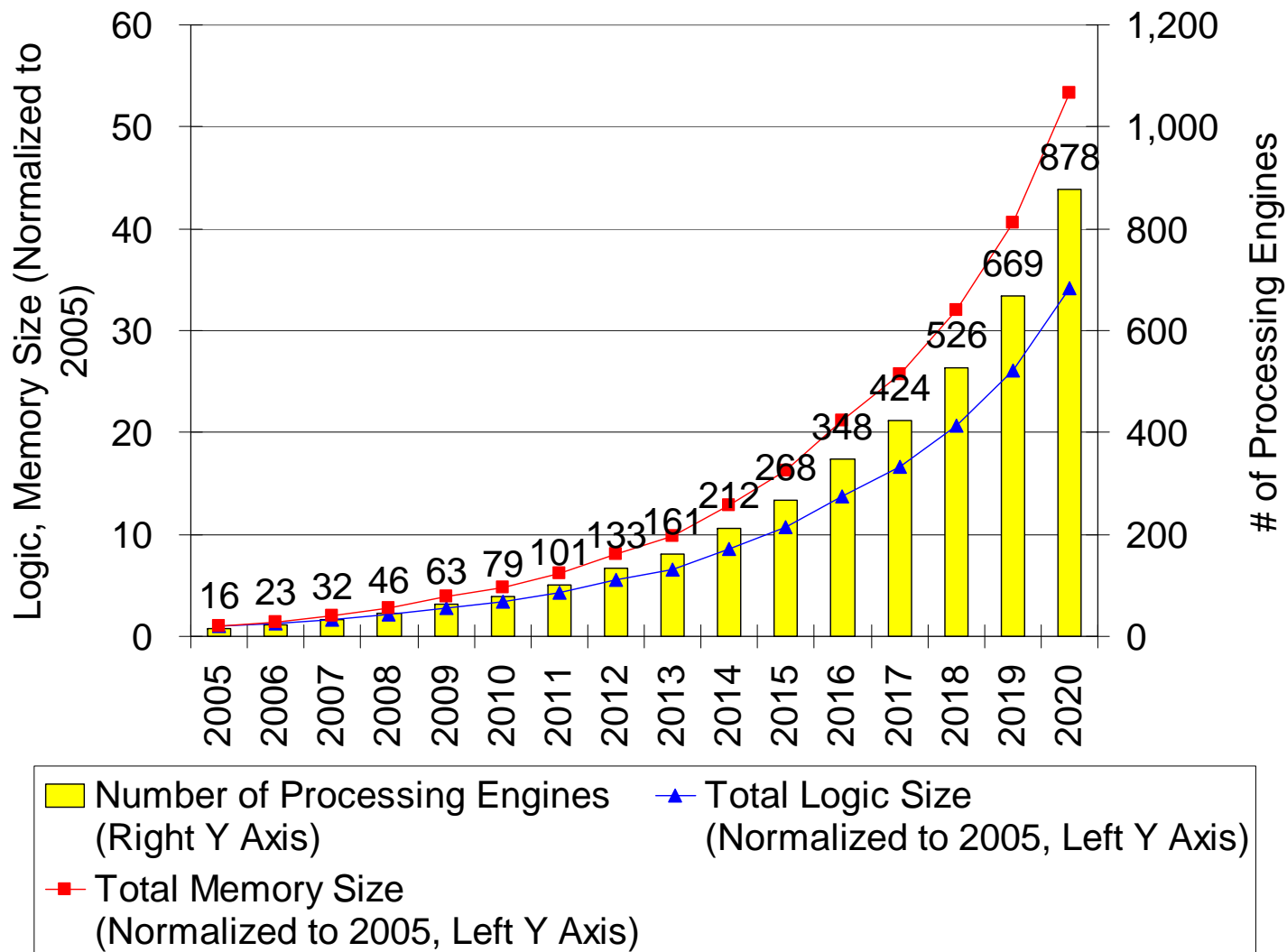


Updated productivity table → **cost**

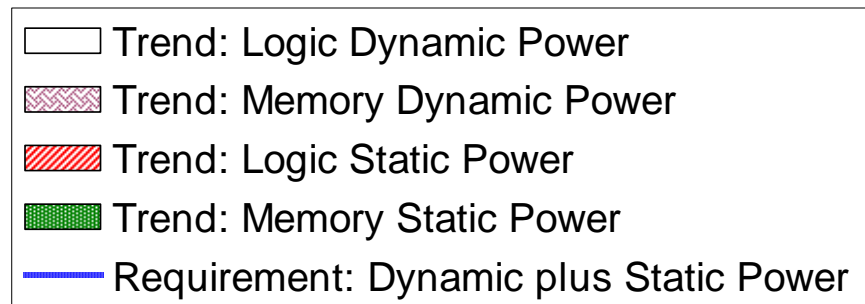
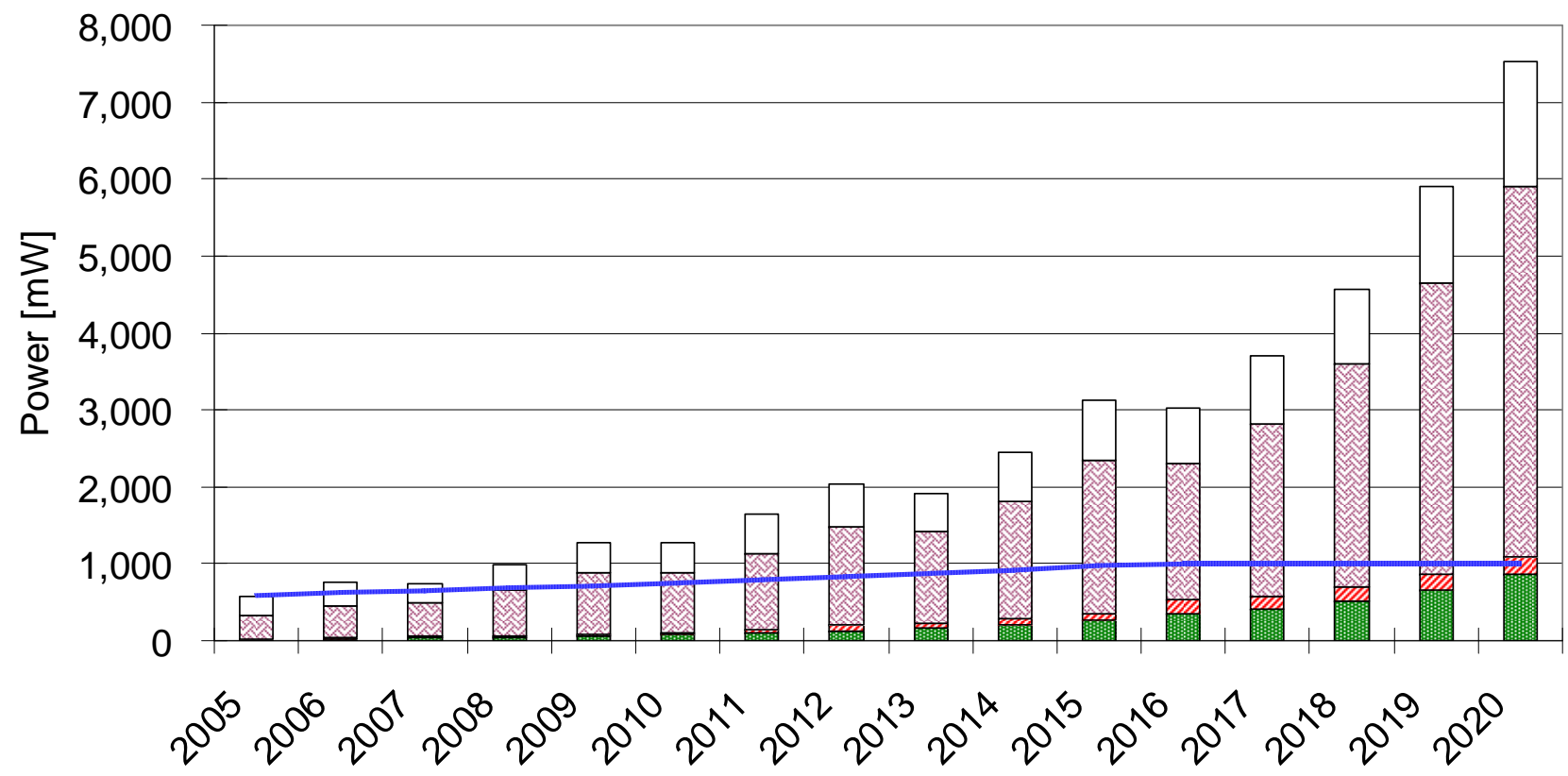
Preserve consistency



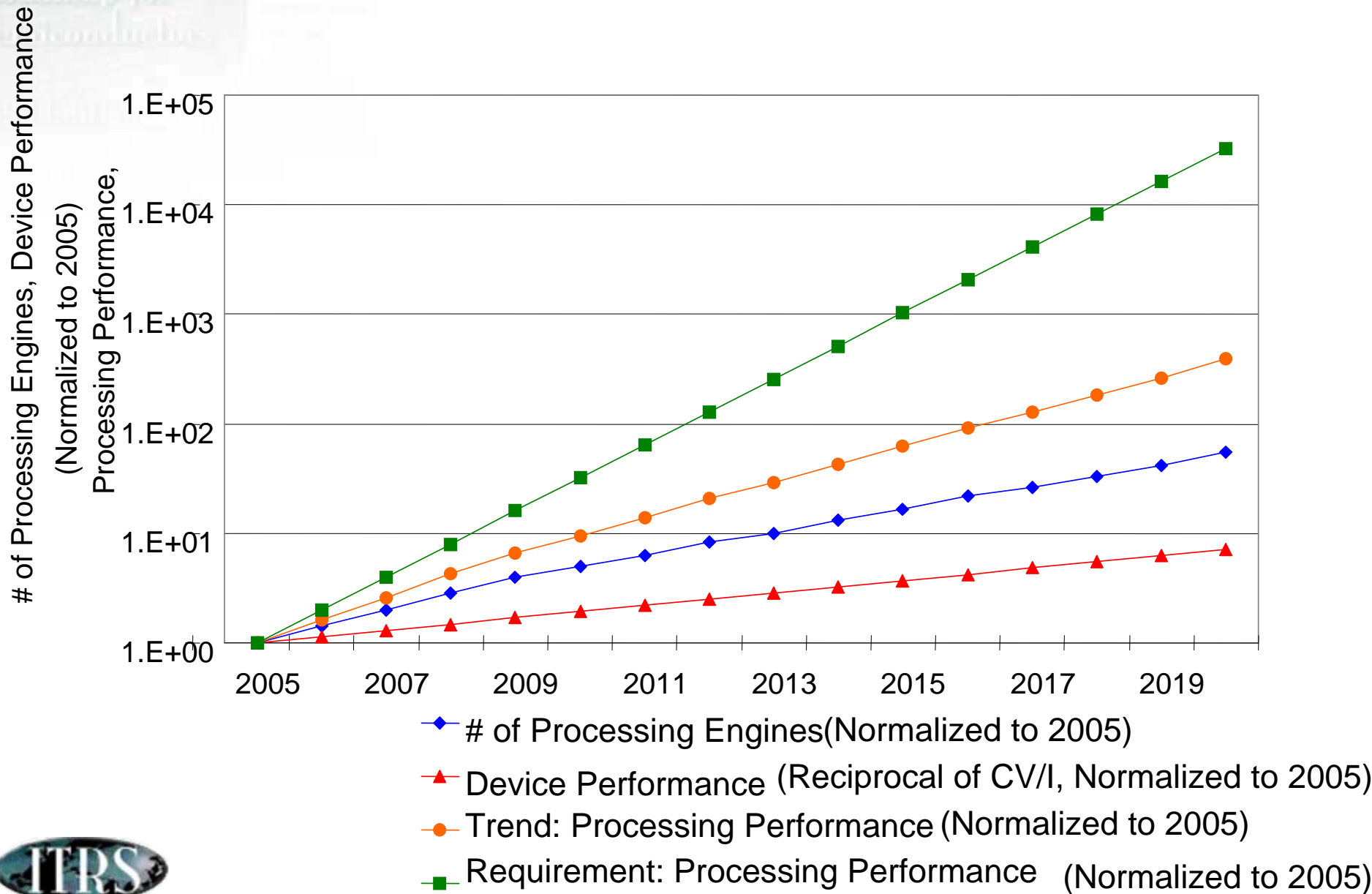
--- Design Complexity Trends (cont.)



--- Power Trends (cont.)



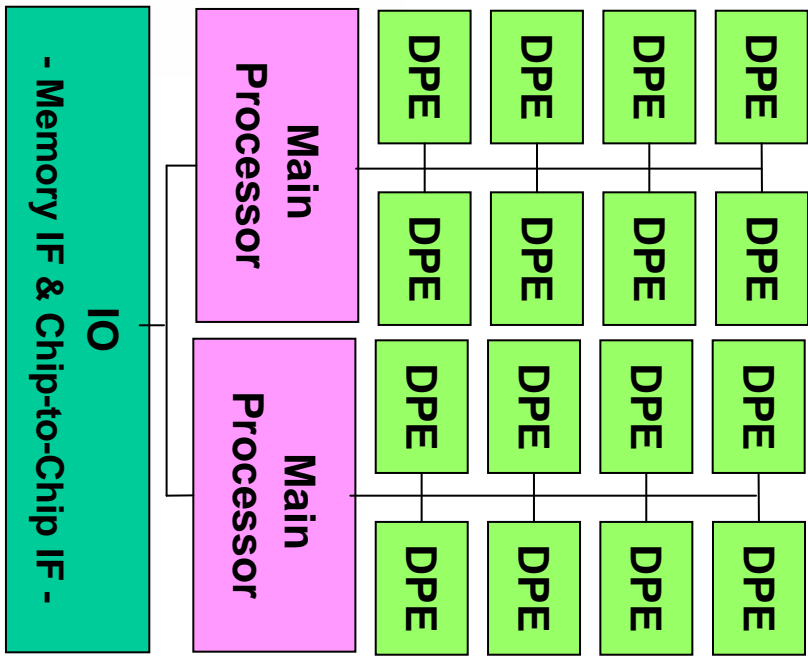
Processing Performance Trends (cont.)



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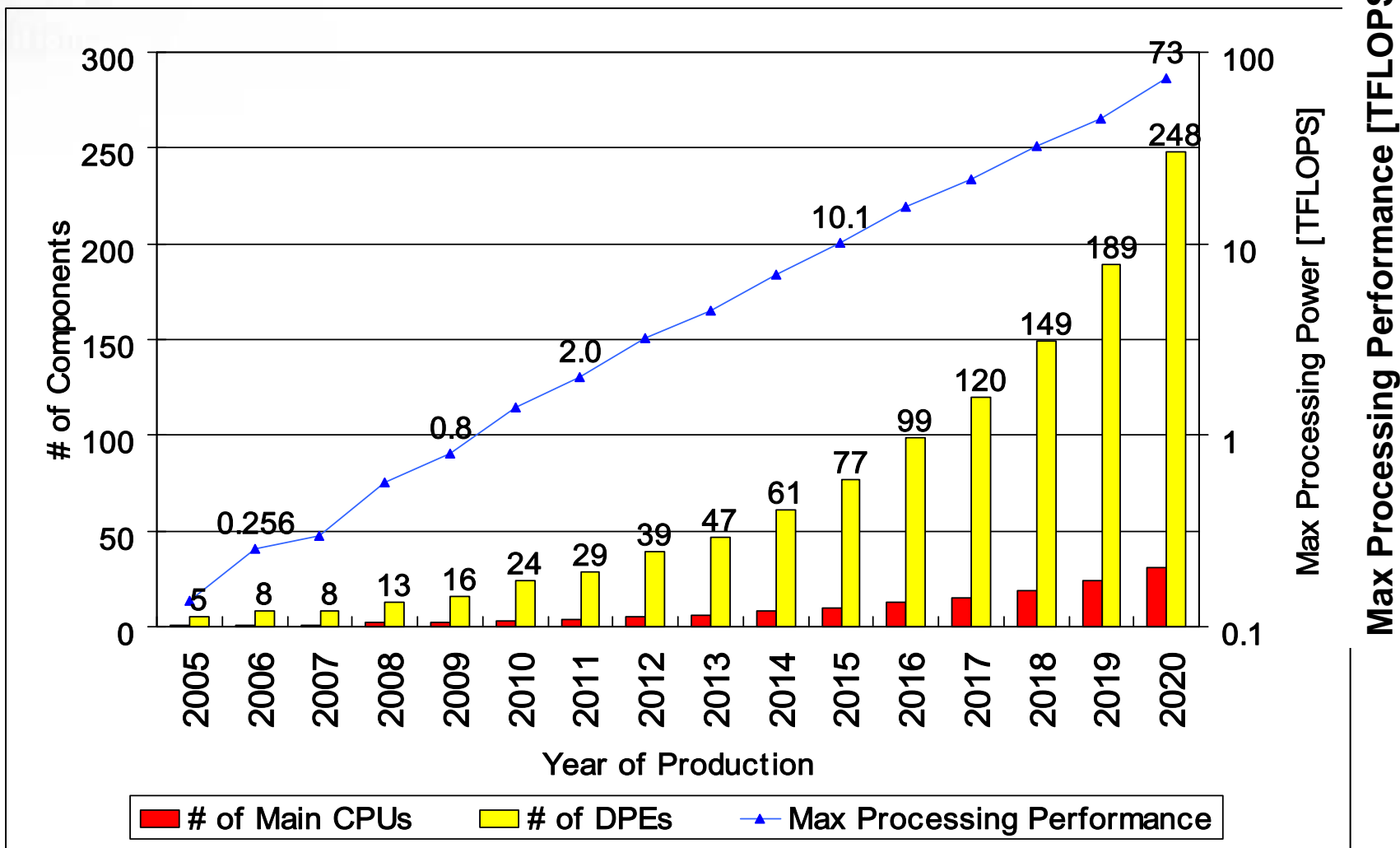
Consumer Driver - Stationary

Architecture Template

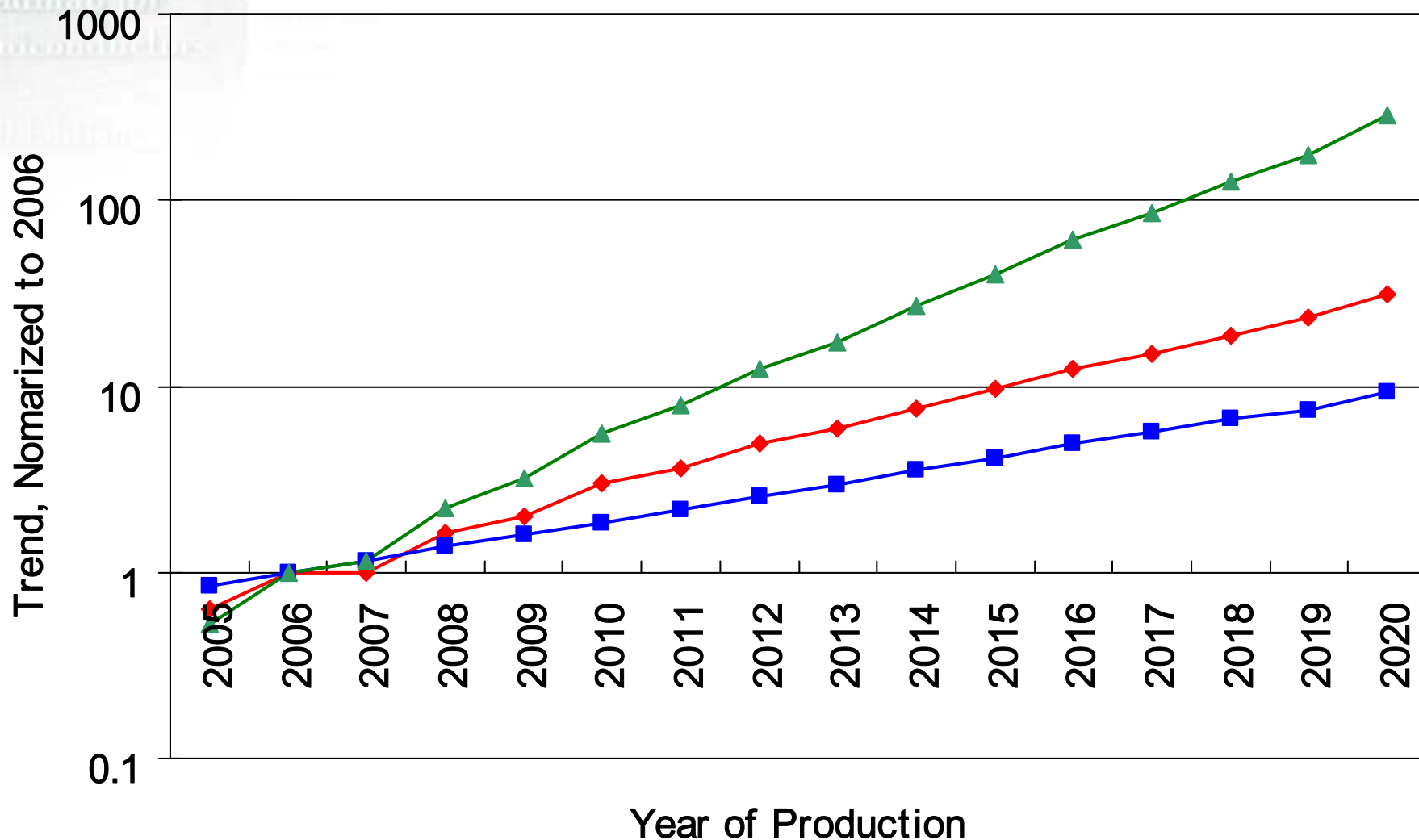


- **SOC die size stays constant around 220mm²**
- **Pair of a Main Processor and a number of DPEs structures basic architecture**
- **Possible largest number of DPEs will be on this SOC to achieve required performance**
- **Circuit size of both Main Processor and DPEs stays constant**
- **A Main Processor is assumed to be able to control up to 8 DPEs**

Design Trend: # of Processors & Processing Performance



Performance Trend



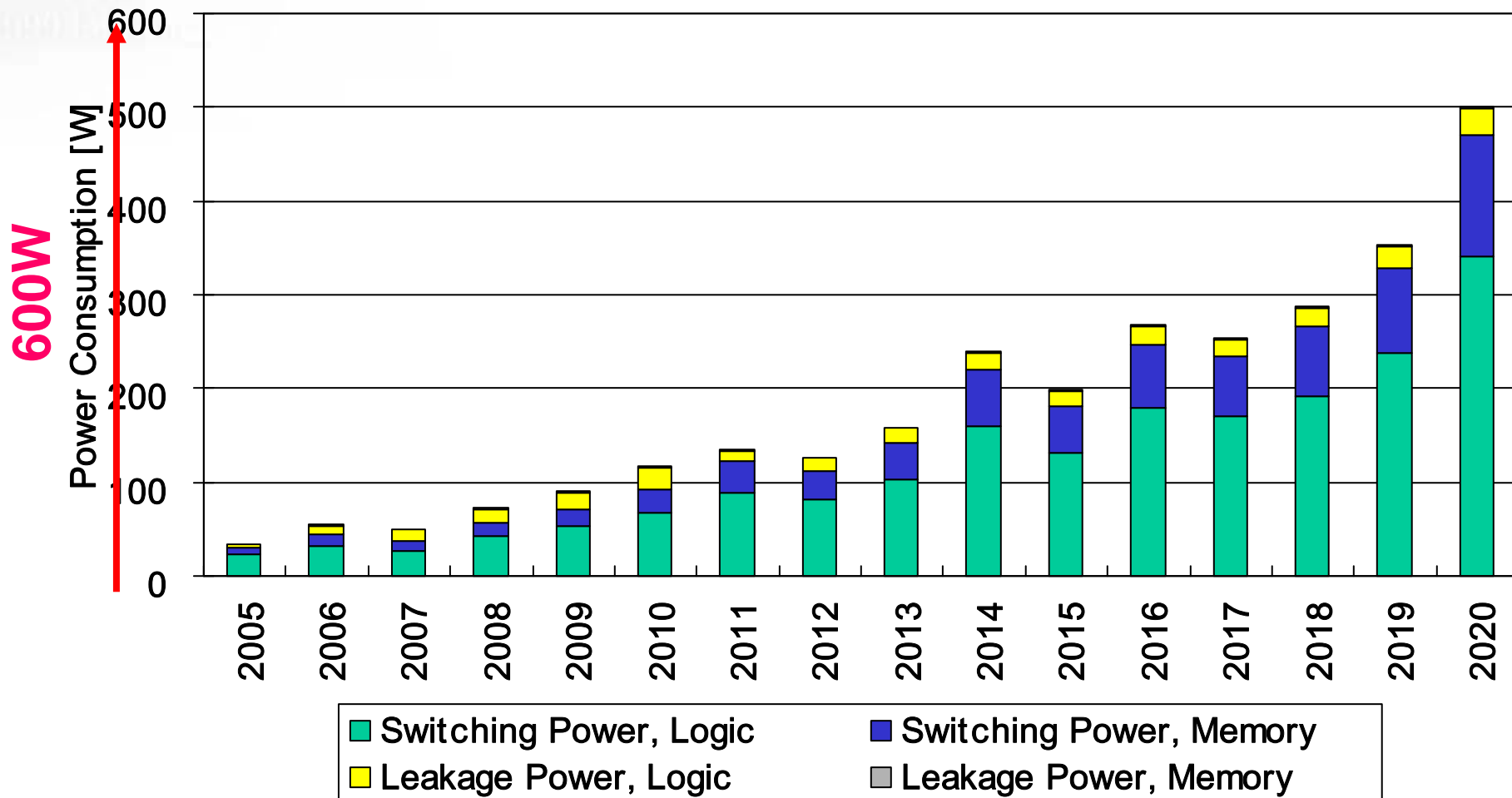
◆ # of DPEs ■ 1/τ : intrinsic switching speed ▲ Processing Performance



Design Trend: Power Consumption

– SOC Total

SOC total power consumption rapidly increases



The New Scaling of Silicon Systems

Networking Driver

New *Networking System Driver*

Multi-Core/Accelerator Engine SoC - Architecture template

Goals

- Performance
- Ease of use

Components

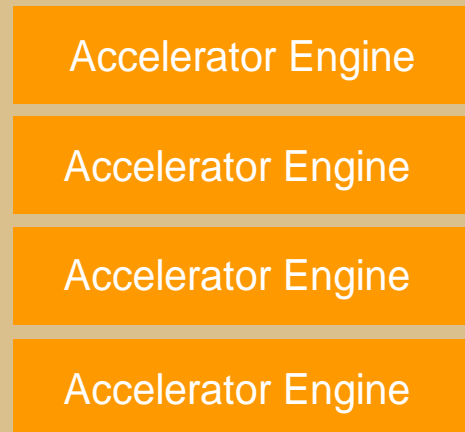
- On-chip fabric
- 32+ cores with private memory
- Accelerator engine app-specific

Multi-Core/Accelerator Engine Platform (SOC-MC/AE Architecture)

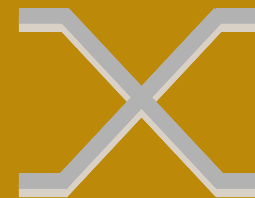
Multi-Cores



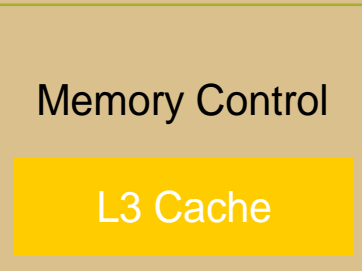
On-Demand Acceleration



Non-Blocking Switch Fabric



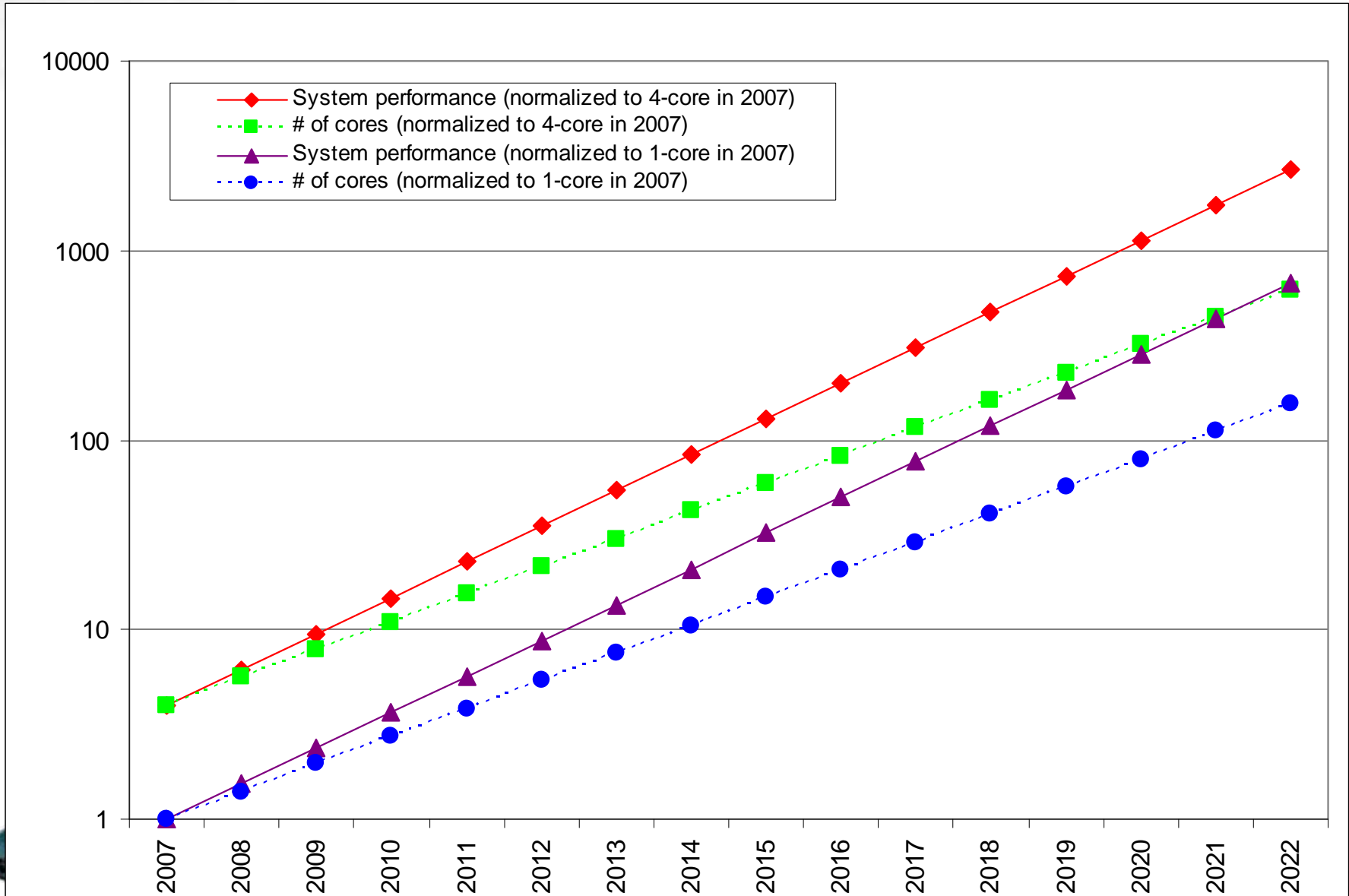
System Functions



Connectivity



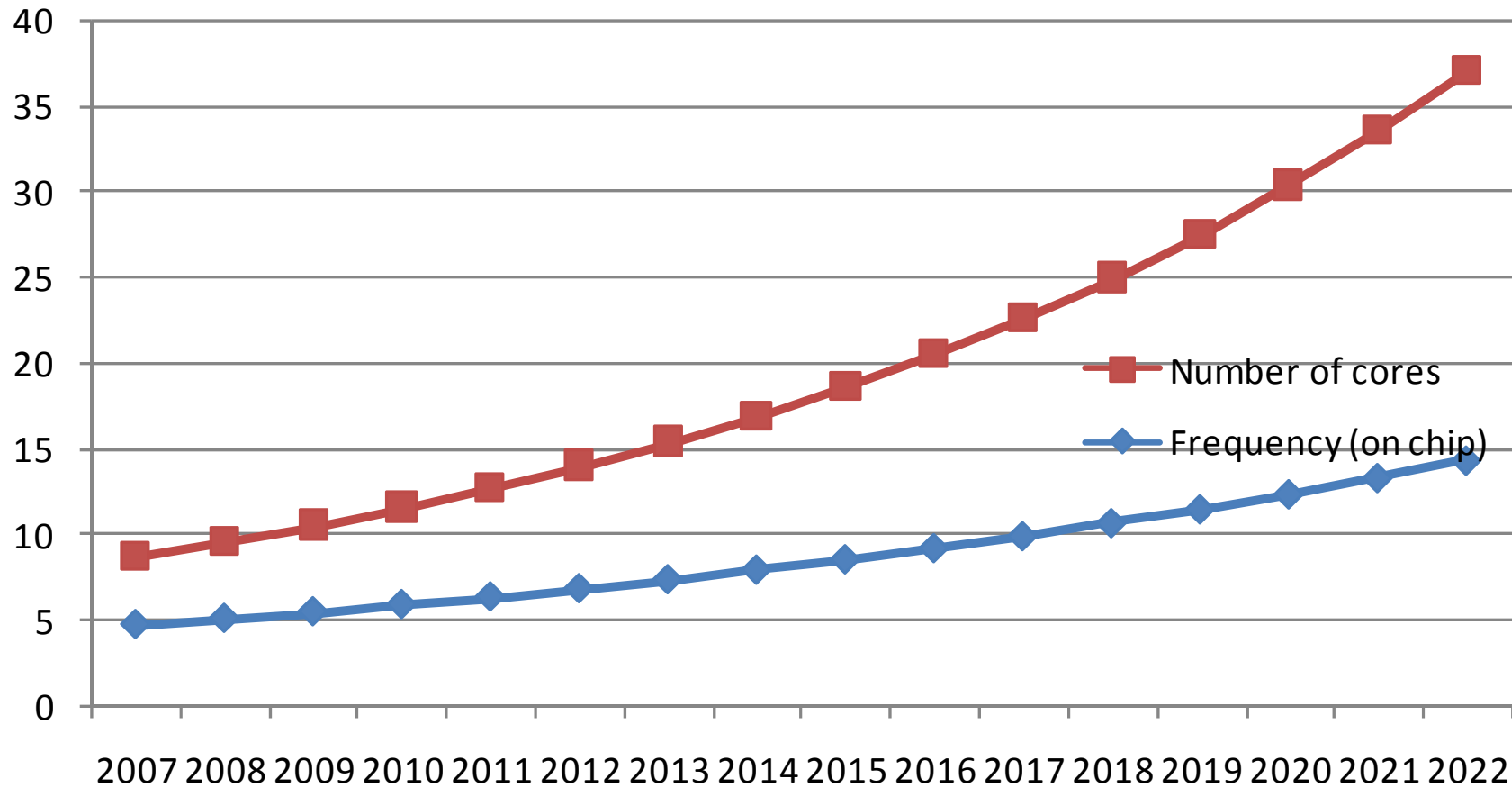
Networking Driver Trends



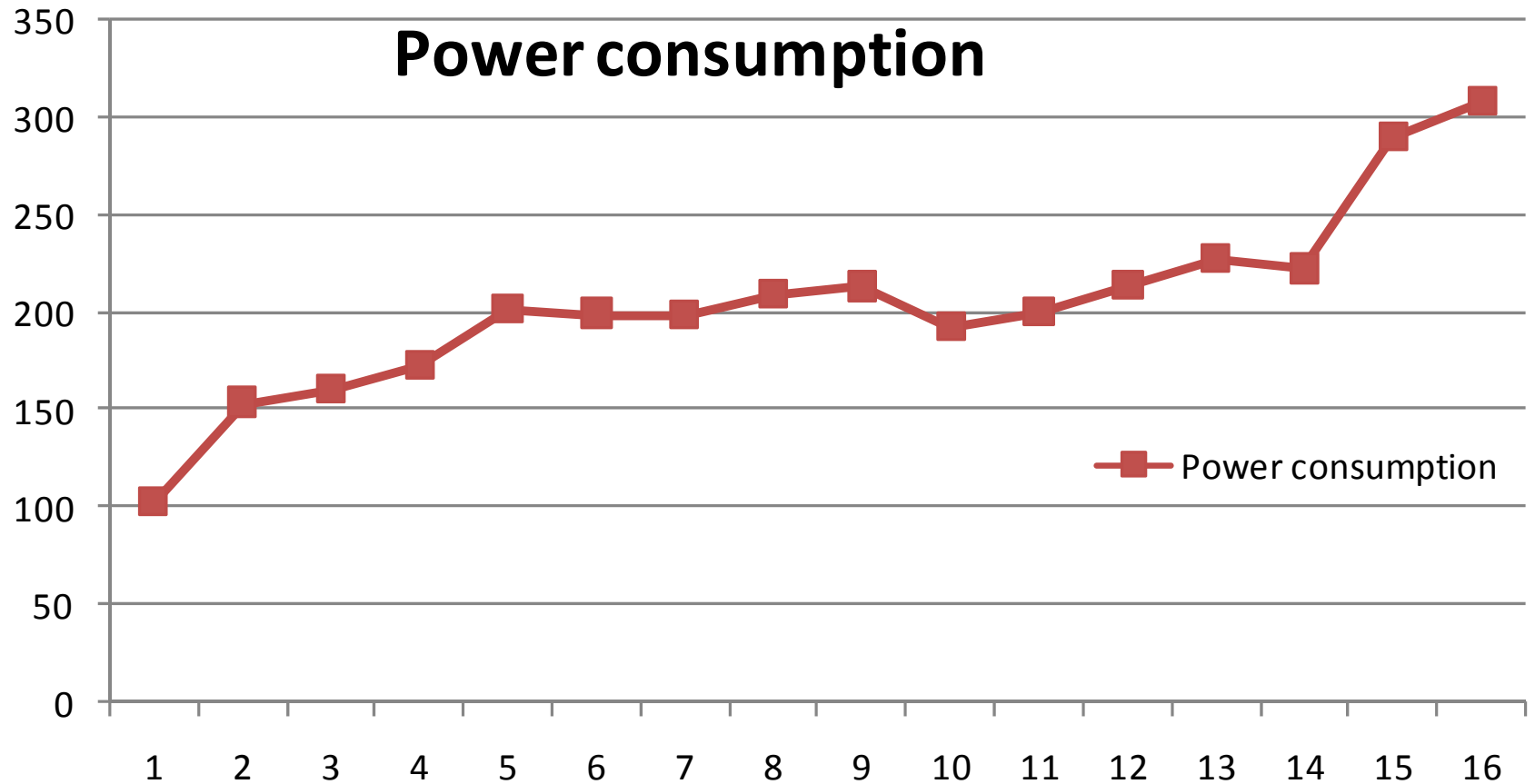
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Office / MPU Driver

Office (MPU) Driver (Updated)

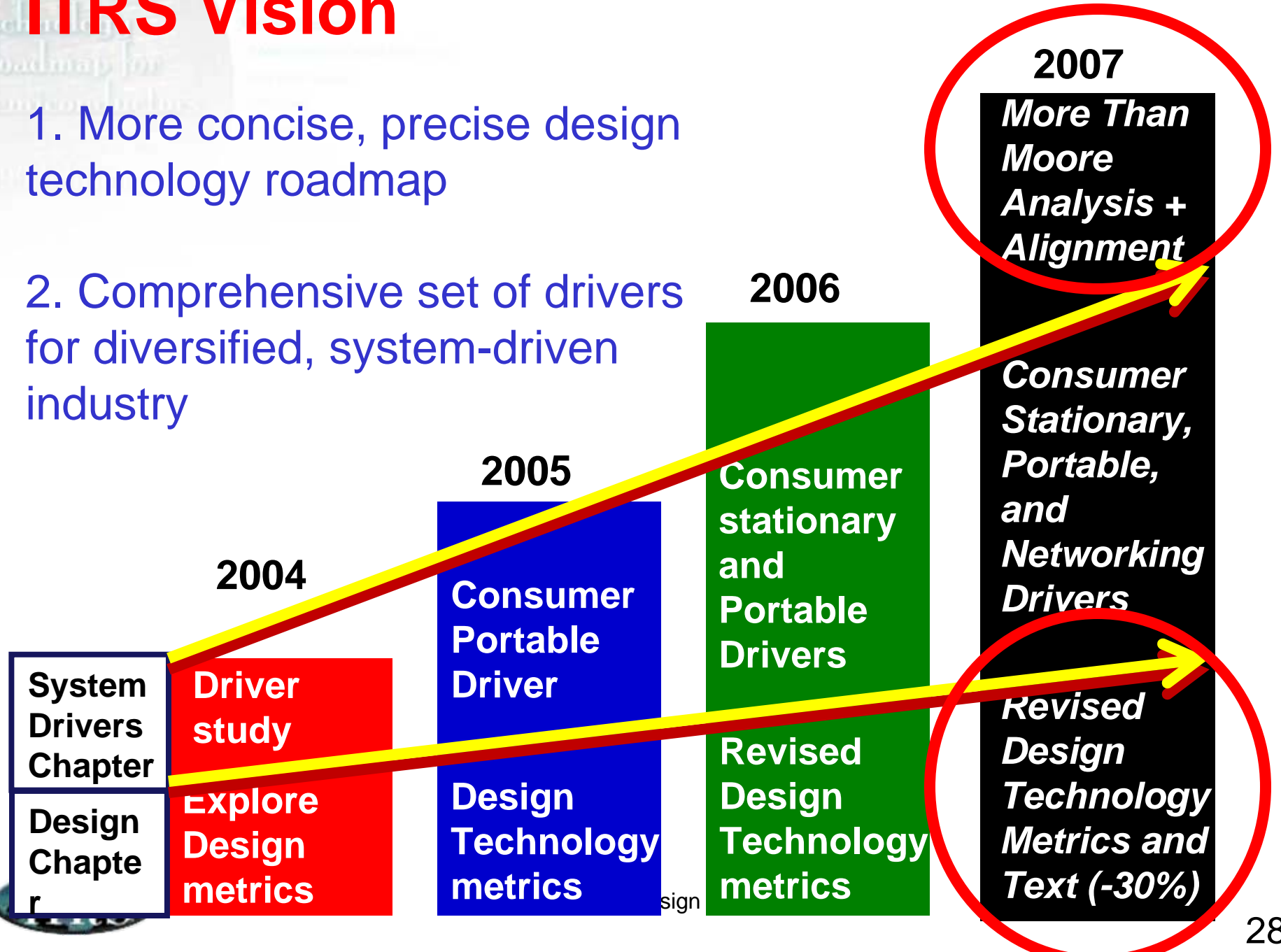


Office (MPU) Driver (Updated)



ITRS Vision

1. More concise, precise design technology roadmap
2. Comprehensive set of drivers for diversified, system-driven industry



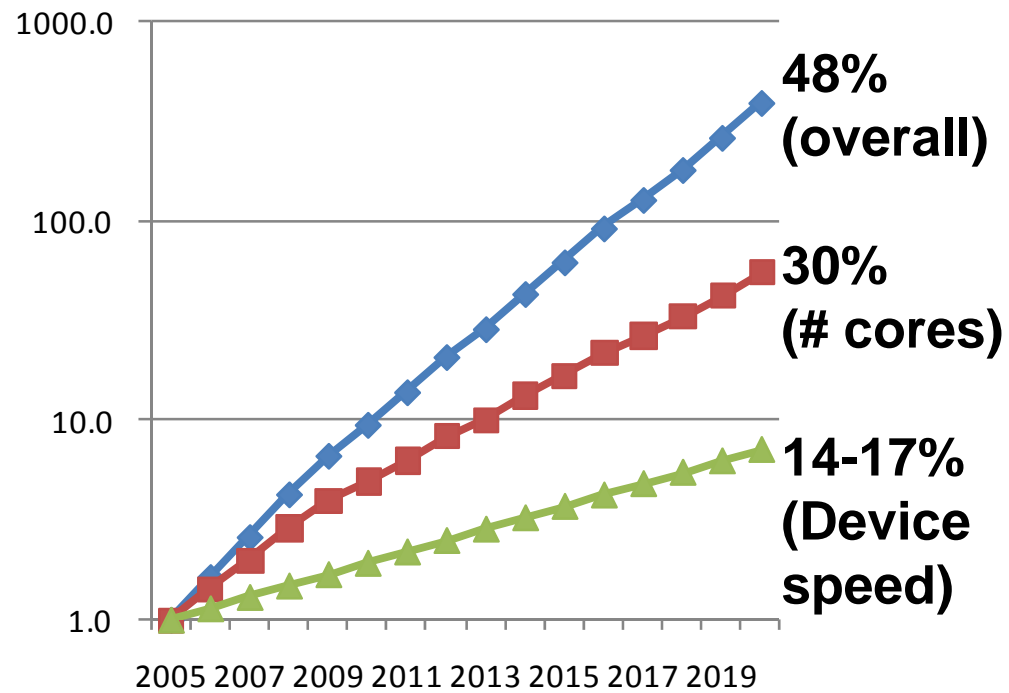
The New Scaling of Silicon Systems

“More Than Moore” Versus “Moore’s Law”

Design-Driven Semiconductor Innovation (Moore Versus “More Than Moore”)

Domain / market independent
Inventory 50+ Design Solutions

Domain / market dependent
(Consumer) driver architecture



- SCALING**
- Moore **Conventional**
- More Moore **Equivalent**
- More Than Moore **Diversified**

ITRS Design TWG 2007

Moore+ Parameter Inventory

Classification of 50+ design technology solutions

1. Supporting Moore's Law – **More Moore (geo scaling)**
2. Extending Moore's Law – **More Moore (equivalent scaling)**
3. Beyond Moore's Law – **More Than Moore (architecture diversification)**

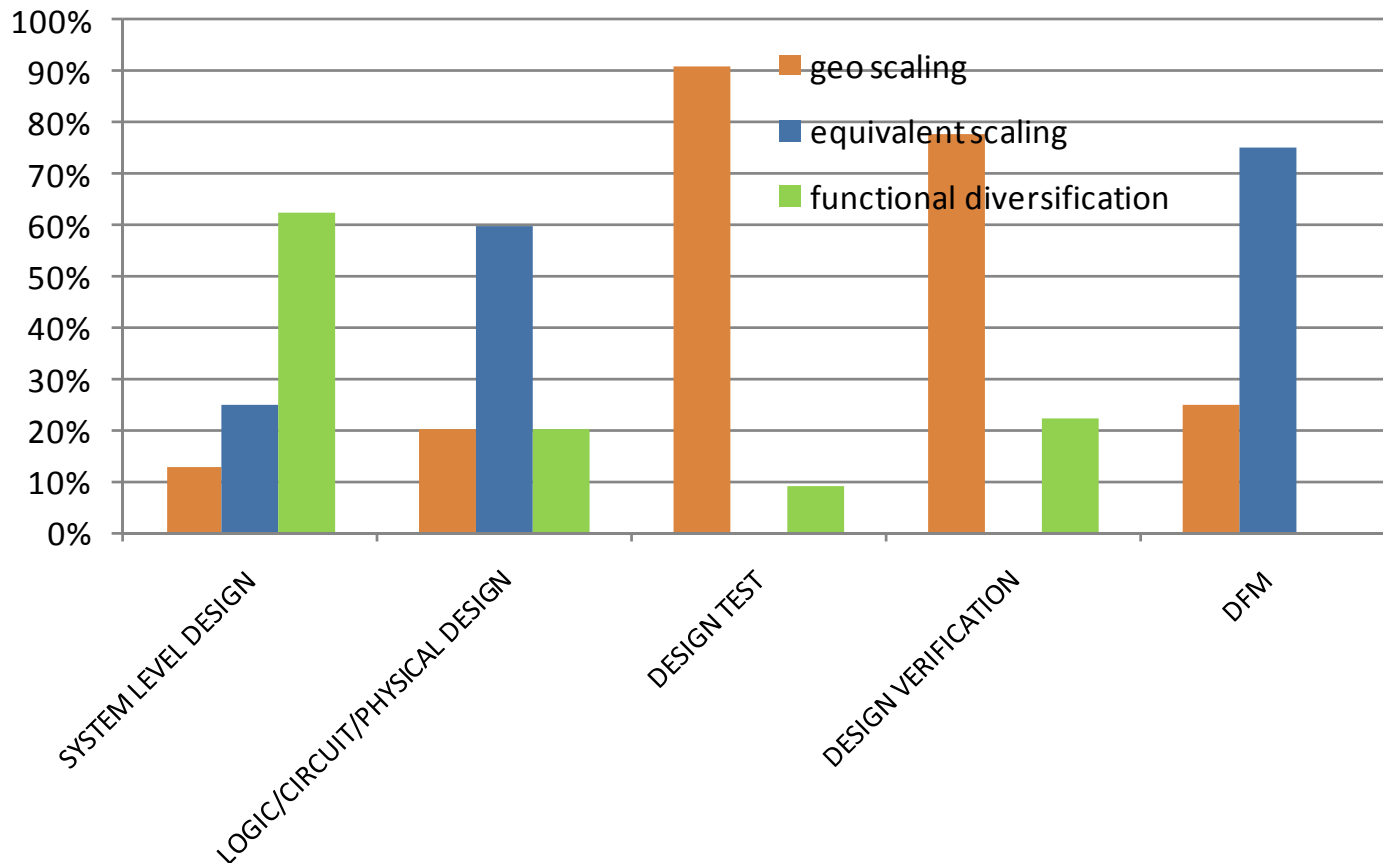
Example: System-Level Design Solutions

	Geometrical scaling	Equivalent scaling	Functional diversification
	Moore	More Moore	More Than Moore
System level component reuse	1		
Chip package co design methods			1
Improved system level power estimation techniques		1	
On chip network design methods	1		
mixed signal / RF verification		1	
automated interface synthesis			1
HW/SW co design and verification			1
Multi fabric implementation planning (AMS/RF/MEMS)			1

Design-Driven Semiconductor Innovation (Moore+)

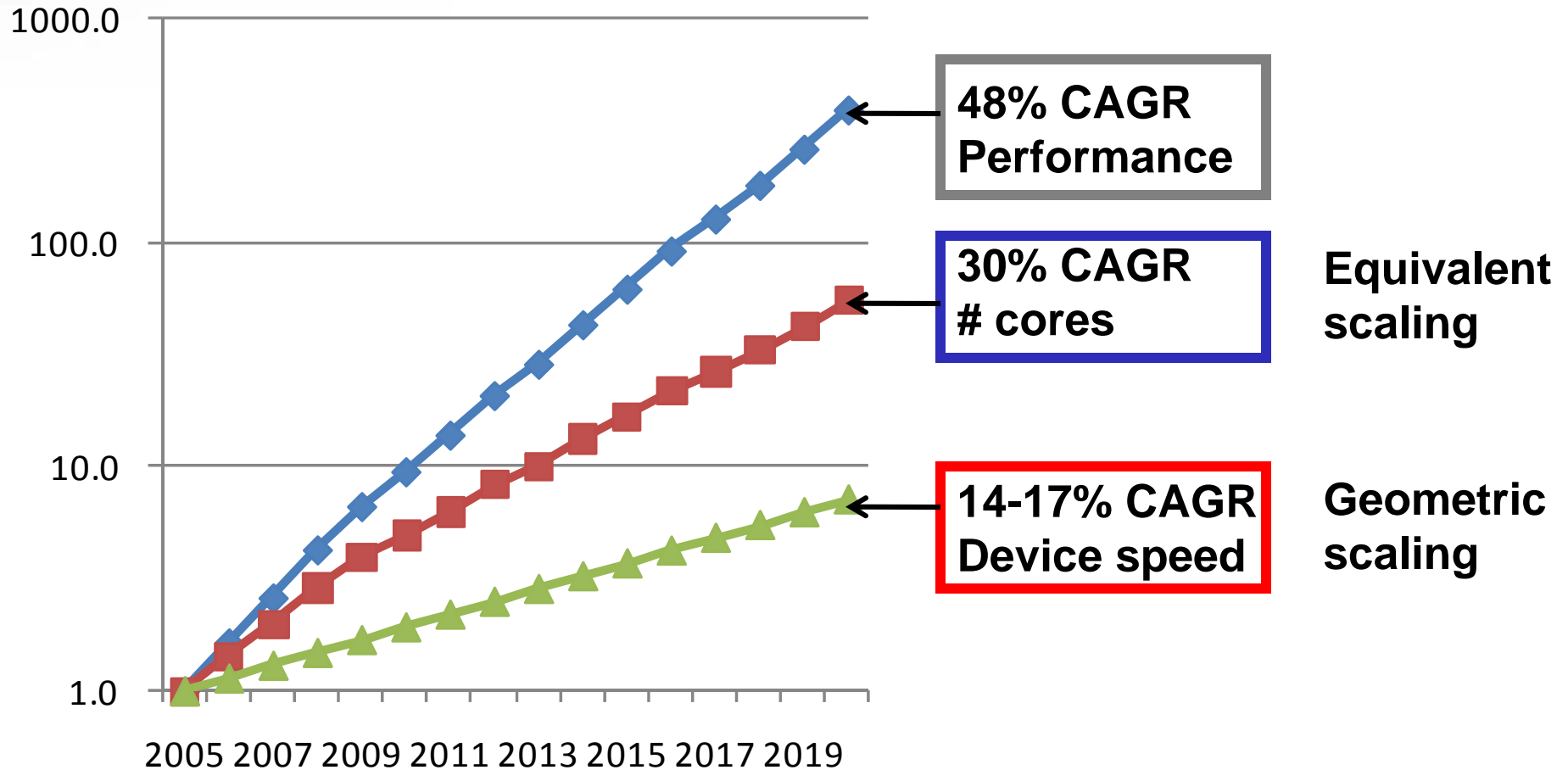
Domain / market independent *Inventory 50+ Design Solutions*

→ Reveals impact of More Than Moore on key design phases



More Than Moore “Pilot Example”

Focused on design levers e.g. multi-core



The New Scaling of Silicon Systems

Direct Alignment between iNEMI and ITRS
→ Consumer Portable Pilot Study

Key iNEMI contact: **Susan Noe**

1st Alignment Between Chip and System Roadmaps

Consumer portable pilot, focused on power/energy

Parameter	COLOR	Metric	2005	2007	2009	2011	2017	Where in ITRS	
Number of Voltages		#						only one (core logic)	
Minimum Logic Family Voltage		Volts	2.5	2	1.8	1.5	0.8	consumer driver	
Maximum Logic Family Voltage		Volts	5	3.3	2.85	2.2	1.8	consumer driver	
Normal Logic Family Voltage		Volts	3.3	2.85	2.2	1.8	1.2	consumer driver	
POWER									
Power		Type	u Polymer, n	u Polymer, n	u Polymer, m	u Polymer, meth	u Polymer, n	NO?	
Spec. energy		Wh/kg	150	175	200	300	400	NO?	
Energy dens		Wh/liter	400	500	550	600	800	NO?	
Specific power		W/kg	1000	2000	4000	5000	6000	NO?	
Shelf life		years	3 years	3 years	4 years	5 years	8 years	NO?	
Avg. standby power		Watts						consumer driver	
Voltage (avg.)		Volts	~10 parameters to be aligned						consumer driver
Voltage (min.)		Volts							consumer driver
Current (avg.)		mA							consumer driver
Run Time Before Recharge		Hours							NO?
Min. and Max. Operating Temperature		Degrees C						NO?	
Max Reflow Temp		Degrees C						NO?	
THERMAL									
Use Ambient Operating Temperature Range		Deg C - Deg C	-10 to 50	-10 to 50	-10 to 50	-10 to 50	-10 to 50	NO?	
Thermal Design Power (Hottest Chip)		Watts	30	40	45	50	60	consumer driver	
Max Current per Device		Amps						consumer driver	
Thermal Design Flux (Hottest Chip)		W/sq. cm						NO?	
Cooling Method		Passive,Active, I	both	both	both	both	both	NO?	
Number of Chips W/Some Heat Sink		# / Assy or Boar						NO?	
Device Cooling Air Temperature (Inside the Box)		Deg C						NO?	
Device Cooling Rail Temperature		Deg C						NO?	
Chips W/ Power < 2W		# / Per Assembl						consumer driver	
Chips W/ Power From 2 - 5 W		# / Per Assembl						consumer driver	
Chipc W/ Power From 5 - 10 W		# / Per Assembl						consumer driver	
Chips W/ Power > 10 W		# / Per Assembl						consumer driver	
Module Power		W / sq. cm.						NO?	

iNEMI-ITRS Power Reconciliation

Top-10 Parameters to be Reconciled

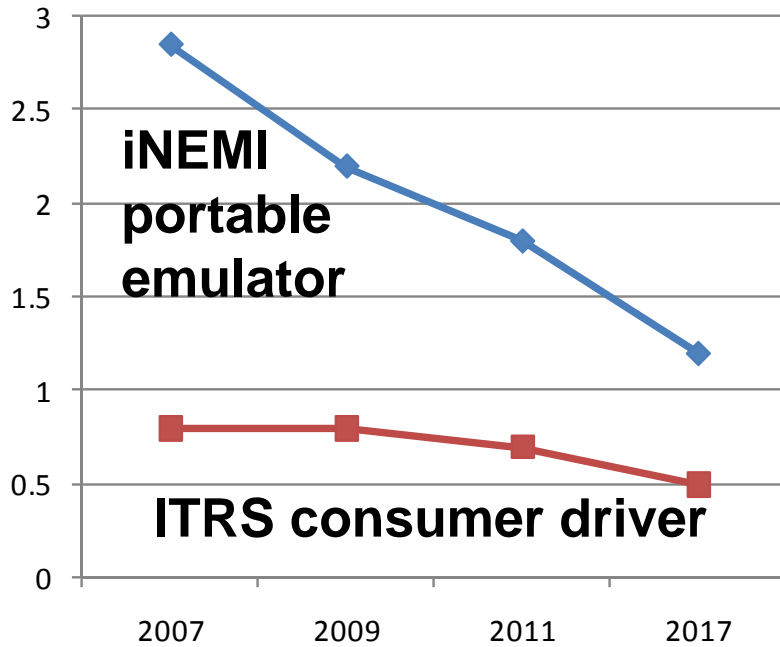
Portable emulator						Consumer portable driver				
iNEMI	iNEMI	iNEMI	iNEMI	iNEMI	iNEMI	ITRS	ITRS	ITRS	ITRS	
iNEMI Parameter	Metric	2007	2009	2011	2017	ITRS parameter	2007	2009	2011	2017
Normal Logic Family Voltage	Volts	2.85	2.2	1.8	1.2	Logic voltage	0.8	0.8	0.7	0.5
POWER										
Spec. energy	Wh/kg	175	200	300	400	N/A				
Avg. standby power	Watts					Total static power	0.052	0.09	0.146	0.58
Run Time Before Recharge	Hours	0.0875	0.05	0.06	0.06667	N/A				
THERMAL										
Use Ambient Operating Temp Range	Deg C - De	-10 to 50	-10 to 50	-10 to 50	-10 to 50	N/A				
Thermal Design Power (Hottest Chip)	Watts	40	45	50	60	total power	0.74	1.281	1.639	3.709
Max Current per Device	Amps					Chip current (P/V)	0.93	1.60	2.34	7.42
Thermal Design Flux (Hottest Chip)	W/sq. cm					N/A				
Cooling Method	Passive,Ac	both	both	both	both	N/A				



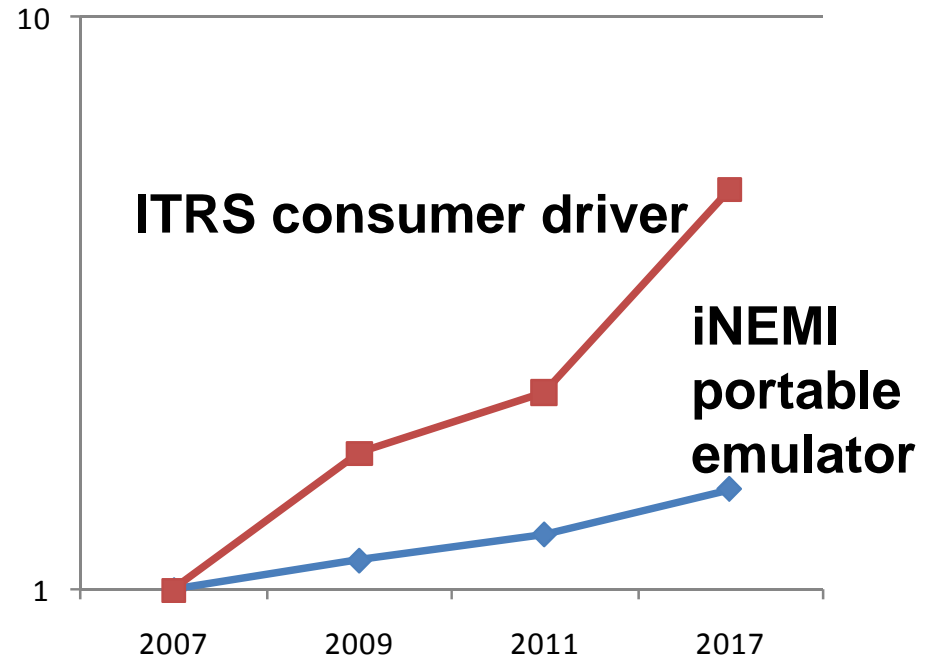
iNEMI VS ITRS (System V. Chip) Power Parameters' Comparison

ITRS stuck between lower voltages and higher power trends

Voltage supply trends

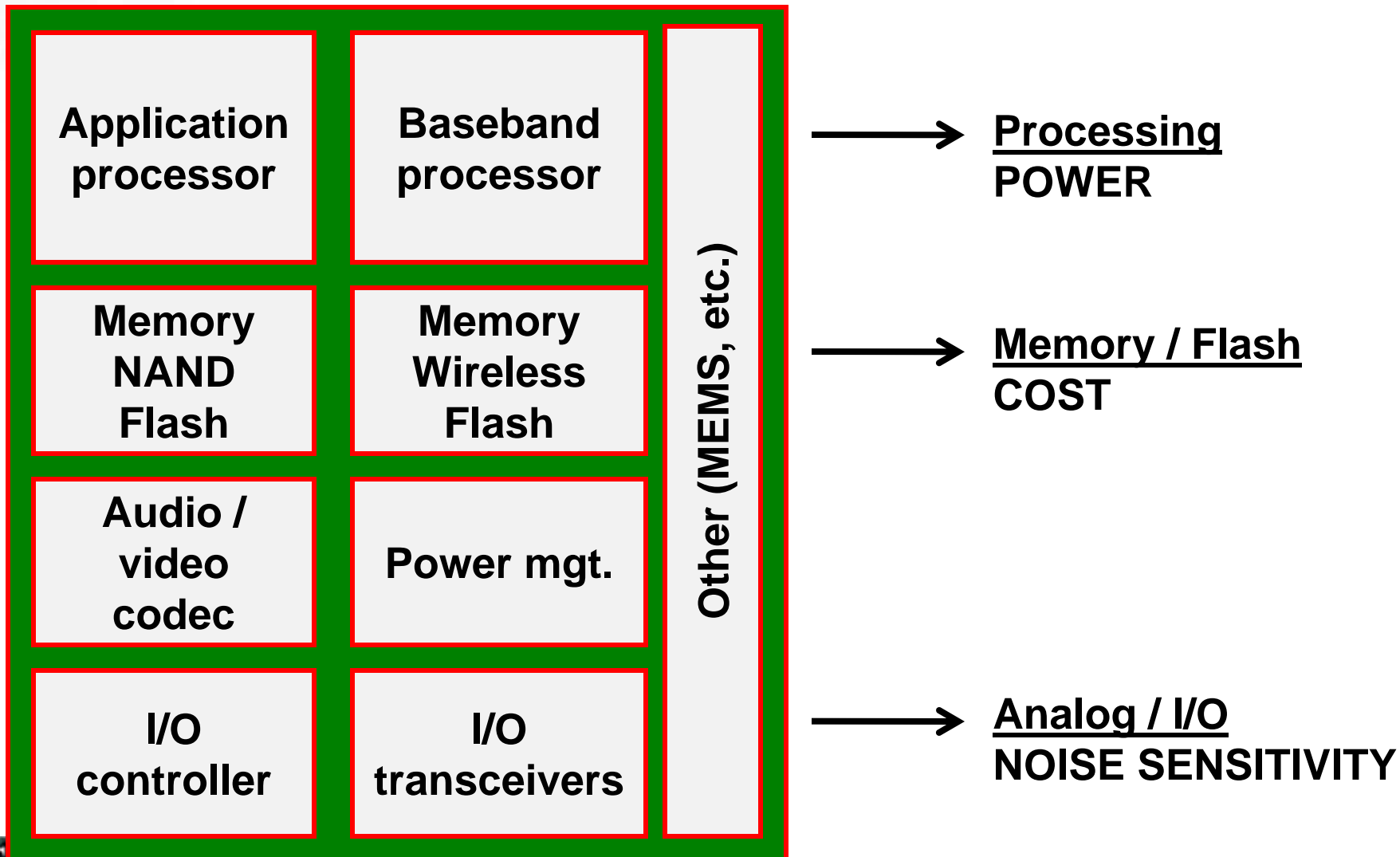


Power trends



Future iNEMI-ITRS

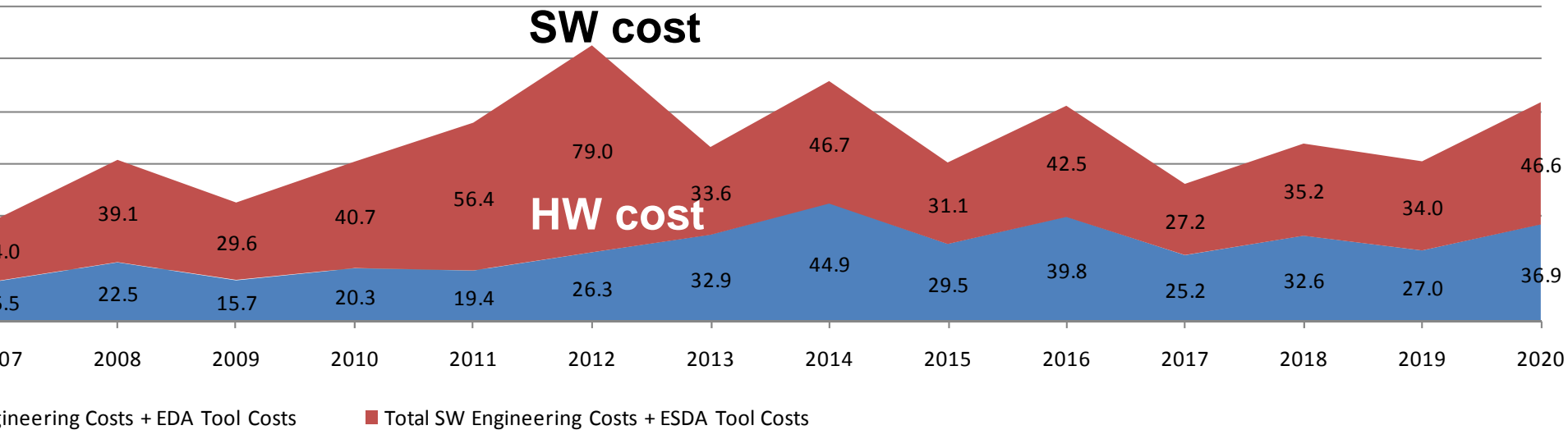
ITRS Portable *System* Model



Current Relevant Activities: Inclusion of New “Fabrics”: *Software*

NRE cost for SW design to equal HW design

→ until design technology for SW issues is addressed



Summary

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Conventional (Moore) + Heterogeneous (Moore+) scaling

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INEMI

Advancing manufacturing technology