2003 NEMI Research Priorities

National Electronics Manufacturing Initiative, Inc.

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Connect with and Strengthen your Supply Chain

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In order to help ensure the ongoing competitiveness of the electronics industry, NEMI continues to focus on improving the manufacturing capability of its member companies. Because the infrastructure required to efficiently provision the customer base is so broad and diverse, the founders of NEMI wisely established a planning methodology to insure that its members could focus on high impact areas that can truly make a difference in the market place. At its fundamental level, that process includes technology roadmapping and technology deployment work. While we continue to refine that process to improve the results, the underlying principals remain unchanged:

1. Create industry roadmaps by drawing upon the expertise of a broad cross section of individuals from industry, academia, and government. The results of this work are open to the electronics industry worldwide.

2. Identify the major areas that NEMI will focus on based on need, participation, and ability to make a business impact.

3. Conduct a gap analysis on these major areas based on the roadmap that identifies the major challenges and opportunities facing the industry.

4. Create five - year plans for the major areas that identify the projects and activities deemed necessary to close the identified gaps. These plans become the basis for the formation of NEMI projects.

While the results of the Roadmapping process provide value to the entire electronics industry, the full measure of value comes from participating in NEMI projects in order to improve the manufacturing capability of member companies. In these efforts, users and suppliers of a particular capability come together to collaborate, in a pre-competitive fashion. Outcomes can take a variety of forms: new processes/equipment, education, standards, tools (both hardware and software). Many of today's projects are driven by improving time to market and reducing the structural cost of the manufacturing supply chain. Those who participate gain the advantage of both influencing the direction and outcome of the project as well as getting a leg up on the competition by achieving early knowledge of the new offering.

This year in addition to the four principles which result in developing a five year plan, we have added a fifth principle: prioritizing the research needs identified in the 2002 NEMI Roadmap. This document is intended to serve as a resource to all who are tasked with directing R&D (both funding and execution). With the downsizing of industrial research in North America, it is critical to encourage academic and institutional R&D centers to focus on technology needs identified in the NEMI Roadmaps. Recent concern in North America over the loss of manufacturing capabilities has stimulated discussion that North America must place greater emphasis on innovation and the development of disruptive technologies. NEMI is committed to improving the roadmapping process to better identify disruptive technologies and research priorities.

On behalf of the NEMI Board of Directors, I congratulate all who helped identify these Research Priorities. More information is available on our web site: www.nemi.org or call us at 703-834-0330.

Sincerely,

Jim McElroy
Executive Director and CEO
National Electronics Manufacturing Initiative, Inc.

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Executive Summary

The 2003 NEMI Research Priorities presents the consensus on R&D needs identified in the 2002 NEMI Roadmap. This document is intended to serve as a resource to all who are tasked with directing R&D (both funding and execution). The individual needs can be understood in the context of the five product sectors (consumer, portable, office systems, large business systems, and automotive/defense) that drive technology and R&D needs. The R&D needs from the 2002 NEMI Technology Roadmap Chapters are organized in five categories: 1) Manufacturing Processes; 2) Energy; 3) Systems Integration; 4) Materials; and 5) Design. Each table item is referenced to its corresponding Roadmap Chapters and Chapter page numbers. Text from the roadmap chapters that specifically addresses R&D needs is also included in its entirety in Appendix A.

A final section on Disruptive Technologies examines how newly discovered phenomena may be exploited in future technologies and lead to R&D needs for the microelectronics industry. In particular, this section describes possible future areas in nanotechnology resulting from the current investment in federal R&D research funding.

It is only through effective prioritization of limited R&D programs that the North American electronics industry will maintain the technology leadership that it has enjoyed for the past fifty years. This 2003 NEMI Research Priorities document has been prepared to aid this prioritization, facilitating more focused investments and an improved rate of return. With a steady stream of research results to harvest, the electronics industry can continue to enjoy growth and prosperity driven by our society's adoption of break-through products that increase productivity and improve lifestyles.

2002 NEMI Roadmap Overview

Introduction

Electronics is the single largest manufacturing employer in North America, and, based on the value of manufactured product, it is the second largest manufacturing industry. Electronics is also an essential input to the competitiveness and productivity of many other sectors of the economy. These include the automotive and aerospace industries, which are becoming increasingly reliant on electronics components for their manufacturing and operational activities.

The Electronics Sub Committee (ESC) under the Civilian Industrial Technology Committee of the National Science and Technology Council worked with the private sector to create the National Electronics Manufacturing Initiative (NEMI). NEMI was established to promote collaborative development by industry, government, and academia of technology and infrastructure required to facilitate manufacture of new, high-technology and electronic products in North America. This initiative, now industry-led, and open to all in the electronics industry, seeks to meet industry goals of improved profitability and global competitiveness.

The structure of NEMI borrows three successful elements from the Semiconductor Industry Association (SIA) and SEMATECH: A road mapping and technology planning process driven by major end users; a council made up of executives/senior managers of electronics manufacturers; and a focus on results, particularly on infrastructure development and deployment. Unlike SEMATECH, however, NEMI relies on a decentralized organization to leverage existing resources within industry and other consortia. The fundamental activities of NEMI include the creation of electronics manufacturing technology roadmaps and the implementation of projects that develop and promote the necessary supply chain infrastructure.

NEMI Roadmap Process

The 2002 National Electronics Manufacturing Technology Roadmap is driven by the five product sectors defined in Table 1. Each product category is characterized by key cost, performance, and technology drivers which were developed by OEMS with a market vision in each sector. The leading electronic systems manufacturers are basing their strategic planning for new products on the assumption that the electronics infrastructure will develop and implement the technology to meet these key drivers. These drivers were then used to develop individual technology roadmaps that identify needed technology.

Table 1. Product Sectors of the 2002 NEMI Roadmaps

Product Sector	Characteristics
Consumer	High volume consumer products for which cost is the primary driver
Portable	Hand held, battery-powered products driven by size and weight reduction
Office Systems	Products which seek maximum performance within a few thousand dollar cost limit
Large Business Systems	High-end products for which performance is the primary driver
Automotive/Defense	Products which must operate in extreme environments

All sectors are looking for smaller and lighter products with increased function and performance that can reliably operate in a wide range of environments. The key variables for each of the sectors are the time to market and price that the customer is willing to pay for the product. The following paragraphs summarize the key drivers by product sector.

Consumer Product Sector Drivers

- High volume products for which cost is the primary driver
- Examples include televisions, portable radios, CD players, and low-end portions of the cell phone and personal computer markets
- Reducing total supply chain cost is a key driver and has led to a distributed supply chain

Portable Product Sector Drivers

- Hand held, battery-powered products driven by size and weight reduction
- Typical products are high-end cell phones, palmtop computers, PDA's, and wireless email or short messaging devices
- The key elements are:
  - Packaging, materials, and processing technology
  - Supply chain optimization
  - Design architecture
- This product sector is a growth market with a demand for increased functionality
- Increased energy storage and power efficiency are gating increased functionality
- The need for rapid introduction of complex, multifunctional new products has favored the development of functional, modular components
- Modular design increases the flexibility and shortens the product design cycle, placing the technology risk and test burden on the producers of the modules

Office Product Sector Drivers

- Maximum performance within a few thousand dollar cost limit
- Examples include low-end servers and high-end personal computers, both desktop and laptop
- Stable market with demand for increased processing and storage performance
- Products have migrated towards legacy-free products
- Supply chain optimization becomes critical for cost control
- A continued focus on shorter, seasonal production cycles

Large Business Product Sector Drivers

- High-end products for which performance is the primary driver
- Characterized by very high performance, high clock frequency, high reliability, and high power density
- Product examples are routers, communications switches, mainframes, scientific computers, servers and cellular base stations
- The market has seen significant erosion particularly in telecommunications and long haul fiber optic systems
- Packaging and design technology has changed from proprietary to commercial
- Materials and component cost reduction are increasingly important
- Material changes for increased performance is a gating item
- Cost-effective communications bandwidth is a key driver with uncertain cost-performance trade-offs between copper, optical, and wireless technologies

Automotive/Defense

- Products that must operate in extreme environments
- Extreme reliability required to meet warranty requirements and mission critical applications
- Sensor and actuator technology are important drivers for new applications
- Product life-cycle and design cycle are significantly longer than for other sectors
- Automotive:
  - Need to respond quickly to environmental legislation and customer specifications is driving a faster design cycle
  - Conversion of analog sensor components to digital will require a systems architecture change to a system that can distribute power at a higher voltage and control commands at a high frequency on a single wire
- Defense/Aerospace:
  - High performance signal processing of sensor data
  - Typical products require both forward and backward traceability as well as stringent control of material and process change
  - The long design cycle and product life cycle is inconsistent with the life cycle for commercial components

The 2002 Roadmaps were developed by eighteen Technology Working Groups (TWGs), in response to inputs from representatives of OEMs in five Product Sectors. These twenty-three groups included more than 369 individuals recruited from over 169 private corporations, consortia, government agencies, and universities. The Product Sectors are defined in the following section. The eighteen TWGs can be classified into five categories:

- Digital Silicon Technology - The driver of the electronics industry
- Business Technologies - Product Lifecycle Information Management (formerly EIT-Enterprise Information Technology, SCM-Supply Chain Management and FIS-Factory Information Systems)
- Design Technologies (Modeling, Simulation, and Design; Thermal Management; Environmentally Conscious Electronics)
- Manufacturing Technologies (Board Assembly; Test, Inspection, and Measurement; Final Assembly)
- Component/Subsystem Technologies (Packaging, Interconnection Substrates - Organic and Ceramic, Passive and RF Components, Optoelectronics, Displays, Mass Data Storage, Energy Storage Systems and Connectors)

Roadmap Meetings were held in Santa Clara and Chicago, and via Web/teleconference. The TWGs presented their progress at the NEMI 2002 Roadmap Workshop in Herndon, VA (NEMI HQ), on June 20-21, 2002. As a result of this process, participants defined industry needs and identified strategic issues.

2003 NEMI RESEARCH PRIORITIES

Introduction

The 2003 NEMI Research Priorities presents the consensus on R&D needs identified in the 2002 NEMI Roadmap. This document is intended to serve as a resource to all who are tasked with directing R&D (both funding and execution). The individual needs can be understood in the context of the five product sectors (consumer, portable, office systems, large business systems, and automotive/defense) that drive technology and R&D needs. The R&D needs from the 2002 NEMI Technology Roadmap Chapters are organized within five research areas:

- Manufacturing Processes
- System Integration
- Energy
- Materials
- Design

The data section of the Research Priorities presents five tables of R&D needs which make the cross referencing of the NEMI Roadmap Chapter information more easily accomplished against the five major research categories. Page references are provided for each of the NEMI chapter headings used in the tables so that the reader can scroll to the appendix and access the source of the information in the table. The 16 Roadmap Chapters' sections referencing R & D needs are included in Appendix A in their entirety. The complete chapters can be accessed in the 2002 NEMI Roadmap available through the NEMI Headquarters website (www.nemi.org). The Highlighted Priorities section attempts to prioritize and highlight the Key Priorities from Each Category:

Summarized Research Priorities by Research Area

<u>Manufacturing Processes</u>

1. More cost-effective electrical test methods
2. More flexible assembly equipment for low volume, high mix, high yield board products, including data driven solder deposition methods
3. Improve technologies for forming and metallization of microvias
4. Assembly processes and equipment that support integrating electronics and optics into single packages
5. Low temperature joining processes for optoelectronics components using multifunctional materials
6. Standard base platforms and process modules for robotic assembly

<u>System Integration</u>

1. Interoperability standards for matching of vendor/supplier hardware for increased competition
2. Improved transport standards to support data protocols
3. The development of compact high heat flux cooling devices
4. SIP package technology requires a new metric for measuring cost effectiveness as opposed to cost per pin
5. Improved MEMS packaging for multichip and 3D applications
6. Technologies such as optical solders and board level waveguides to enable more complex and higher density board level products
7. Low cost standardized testing for use both in manufacturing and in the field

<u>Energy</u>

1. Lower Voltage components and assemblies
2. Higher energy density/specific energy power supplies, batteries, and fuel cells

<u>Materials</u>

1. Substrate materials with improved dimensional stability, planarity, low moisture absorption, and warpage
2. Improved interfacial adhesion and strength between Cu/low k and wire bonds, bumps, and underfill
3. Low loss resins for high frequency applications

4. Cost-effective, reliable, environmentally conscious material alternatives that meet functional and performance requirements
5. Multifunctional materials for low temperature joining of optoelectronics components
6. Low cost, higher thermal conductivity packaging materials

Design

1. Improved design tools for optoelectronics, MEMS, and other emerging technologies
2. Integrated design and simulation tools needed for mixed mode wireless chips and modules
3. Design for Manufacturing and Disassembly tools needed to address environmental, health and safety issues in addition to manufacturing
4. Improved thermal management designs to reduce power consumption and keep optical components within operating ranges
5. Experimental tools capable of measuring electrical, thermal, and mechanical material properties at smaller scales
6. Integration of optics and electronics in PWB design methodology

Research Priorities by Research Area

The following sections further elucidate specific research needed by 2007. Within each research area, the needs are further organized into Technology Working Group (TWG) lists. Further explanation is provided in Appendix A, which is organized by TWG.

Manufacturing Processes

- **Board Assembly:**
  - Multifunctional materials for low temperature joining of optoelectronics components
  - High yield fiber handling automation systems for optoelectronic assembly
  - More flexible assembly equipment for low volume, high mix, high yield board products, including data driven solder deposition methods
  - Improved aqueous cleaning processes for high I/O, large components and lead-free processing
- **ECE:**
  - DfM tools needed to address manufacturing, health and safety issues
- **Final Assembly:**
  - Standard base platforms and process modules for robotic assembly
  - Software interoperability standards needed for final assembly equipment
- **Interconnect Substrates – Ceramic:**
  - Photo patterning to create high-density spirals for inductors
  - Processes for producing smaller vias
  - Improved mask technology and alignment for finer line widths and dimensional control
- **Interconnect Substrates – Organic:**
  - Laser direct imaging/writing
  - Resistless processes
  - More cost-effective electrical test methods
  - Improve technologies for forming and metallization of microvias
- **Optoelectronics:**
  - Component packaging standards for emerging applications based on reliability, scope and usability
  - New reliability standards that differentiate between telecommunication backbone networks and datacom and premise applications
  - Assembly processes and equipment that support integrating electronics and optics into single packages

System Integration

- **Final Assembly:**
  - High yield at system level

  - Design for automated assembly and disassembly (Design for Manufacturing)
- **Connectors:**
  - High speed copper cable connectors for high speed loss compensation
- **Mass Data Storage:**
  - Semiconductor lasers with shorter wavelengths and optical lens configurations with higher numerical apertures for optical storage devices
- **Optoelectronics:**
  - Interoperability standards for matching of vendor/supplier hardware for increased competition
  - Low cost standardized testing for use both in manufacturing and in the field
  - Improved transport standards to support data protocols
  - Technologies such as "optical solders" and board level waveguides to enable more complex and higher density board level products
- **Packaging:**
  - Improved MEMS packaging for multichip and 3D applications is required
  - The SIP package technology requires a new metric for measuring cost effectiveness as opposed to cost per pin
- **Test, Instrumentation, and Measurement:**
  - Compliant arrays with hybrid probes using E-field and H-field to improve resolution and reduce analytical ambiguities
  - Develop at-speed methods of functionally stimulating units under test, through advanced signal injection techniques Integrated, affordable probe array software system to detect, isolate, and evaluate faults rapidly for a wide spectrum of electronics
- **Thermal Management:**
  - Develop compact, high heat flux cooling devices has been identified by federal government research agencies

Energy

- **Energy Storage Systems:**
  - Lower Voltage components and assemblies
  - Higher energy density/specific energy power supplies, batteries and fuel cells

Materials

- **Board Assembly:**
  - Higher performance materials
  - Low cost, high temperature materials compatible with lead-free reflow to widen process windows for board assembly and rework
  - Multifunctional materials for low temperature joining of optoelectronics components
- **Connectors:**
  - High speed/high density backplane connectors
  - Parallel optical connections
  - High I/O land grid array sockets
  - High performance memory sockets

- **ECE:**
  - Cost-effective, reliable, environmentally conscious alternatives to materials of concern that meet functional and performance requirements
- **Interconnect Substrates – Ceramic:**
  - Lower K dielectric materials needed for high speed digital signal applications
  - Thick film resistor and higher K capacitor materials compatible with LTCC tapes
  - Stable N2-fired resistor materials system
- **Interconnect Substrates - Organic and Packaging:**
  - Low loss resins for high frequency applications
  - Improved materials for embedded resistors, capacitors, and inductors

  - Improved preservative materials for bare copper boards
  - Substrate materials with improved dimensional stability, planarity, low moisture absorption, and warpage
  - Higher density, lower cost substrates
  - Improved underfills for flip chip on organic substrates
- **Mass Data Storage:**
  - Materials, processes, and design for perpendicular and patterned recording media, tunneling magnetoresistive heads (TMR), and heat-assisted magnetic recording (HAMR)
  - Improved subcomponents and materials supporting higher volumes
- **Optoelectronics:**
  - Lower cost optical components such as SOAs, VCSELs, and semiconductor switch products
  - Development of photonic crystals or other materials that are amenable to size scale reduction (compared to Moore's Law for electronics)
- **Packaging:**
  - Improved interfacial adhesion and strength between Cu/low k and wirebonds, bumps, and underfill
  - Lead-free, Antimony-free, and halogen-free packaging materials required to meet new environmental requirements
- **Integrated Passives:**
  - Achieve manufacturable 0.3 uF/cm^2 for organic substrates
  - Develop high ohms/square thin film resistor materials
  - Solve the problems with PTF resistors
  - Improve the yield and reliability of large area thin film embedded caps
- **PLIM:**
  - R&D is needed to develop ways to raise IT system performance levels, harmonize data, and create/exchange standardized decision support information.
- **Thermal Management:**
  - Low cost, higher thermal conductivity, packaging materials, such as: adhesives, thermal pastes, and thermal spreaders need to be developed for use in products ranging from high performance computers to automotive applications
  - A need for high performance, compact, cost effective and reliable cooling systems
- **RF Components:**
  - Medium power, low loss, high selectivity filters are a cost, weight and size bottleneck to Consumer and Portable products and need a solution
  - Improvements in RF filter technology are not occurring rapidly enough to meet the cost/performance demands of both the Portable and infrastructure product sectors
  - The rate of improvement in ADC technology is not fast enough to meet the implementation of digital linearizers in Portable units

Design

- **ECE:**
  - Cost, LCA, and DfE tools needed to address “triple bottom line”
  - DfM tools needed to address health and safety issues in addition to manufacturing
- **Interconnect Substrates - Organic and Packaging:**
  - Improved design tools for optoelectronics, MEMS, and other emerging technologies
  - Coordinated design tools and simulators for chip, package and substrate co-design
- **Mass Data Storage:**
  - Recording channel and preamplifier design, dual actuator servo system design, and advanced motor and actuator design
  - Increased servo bandwidth, possibly using MEMS
- **Modeling Simulation and Design Tools :**
  - Robust tools to predict and optimize performance of optoelectronic substrates
  - Integration of optics and electronics in PWB design methodology
  - Experimental tools capable of measuring electrical, thermal and mechanical material properties at smaller scales

- **Optoelectronics:**
  - Improved thermal management design to reduce power consumption and keep optical components within in operating ranges
- **Integrated Passives:**
  - Need to determine the amount and distribution of capacitance required for decoupling with integrated capacitors
- **Thermal Management:**
  - Integrated mechanical, electrical and thermal package/product design
- **RF Components:**
  - Improved antenna design needed for software defined radios, dual band , dual mode radios and other portable products
  - Integrated design and simulation tools needed for mixed mode wireless chips and modules

Disruptive Technologies

Overview

The roadmapping process does not explicitly identify disruptive technologies, but by identifying needs, particularly those for which there are no known solutions that meet the performance and cost requirements, they implicitly identify areas for innovation and the utilization of disruptive technologies. As an example, the first NEMI Roadmap in 1994 determined that the introduction of area array packaging created a need for new substrate technology. Recent concern in North America over the loss of manufacturing capabilities to China has stimulated discussion that North America must place greater emphasis on innovation and the development of disruptive technologies. NEMI is committed to improving the roadmapping process to better identify disruptive technologies. As we move beyond the digital convergence of many electronic products, we anticipate the merger of micro and nano chemical, mechanical, and biological sensors with micro and nano electronics for disruptive products in many areas.

These breakthroughs may take the form of disruptive technologies that supplant existing technologies. Examples of these are quantum computing systems, molecular electronics, and spintronics replacing CMOS semiconductor technology. Others may be radically new applications, such as sensor and drug delivery systems that detect emerging disease in the body or treat existing diseases. Such personal healthcare systems would give an added dimension to the NEMI consumer and portable product sectors.

Nanotechnology

The rapidly increasing functionality and availability of microelectronics have combined over the last five years with new discoveries in the physical and biological sciences to create public demand for systems that dramatically increase the quality of life. One manifestation of this public demand in the United States is the National Nanotechnology Initiative (NNI).

The National Nanotechnology Initiative's definition of Nanotechnology is "working at the atomic and molecular and supramolecular levels, in the length scale of approximately 1-100 nm range, in order to create materials, devices and systems with fundamentally new properties and functions because of their small structure".

Nanotechnology in its various forms has strong implications for NEMI members and the competitiveness of the North American electronics industry as a whole. Currently, academic, government and start-up company developments put the USA in a strong, but not dominant, technology position world-wide. The projected US Government support of $710M in 2003 represents approximately 30% of global spending in nanotechnology R&D.The Canadian support for nano-technology in 2003 is estimated to be $36.3M. It is widely recognized that there is the potential to grow significant businesses based on nano-formed materials and structures. Some estimates predict a $1 trillion per year industry in the 2010-2015 time frame; as large as the automobile industry or electronics industry.

There are several examples of nano-materials in commercial use today in the electronics industry, including carbon black and ultrafine silica. The semiconductor industry is already in the nano realm and nano-structured materials include the latest generation of sub-100 nm ICs and thin-film GMR (giant magnetoresistive) high density disk drive heads. Micro-crystalline hydrothermal barium titanate capacitor raw materials have been available for more than ten years.

Materials based on nanotechnology can exhibit anomalous chemical, mechanical, electrical or optical products relative to their "bulk" counterparts. These may be useful as-is or as precursors for other useful materials. For example, barium titanate from hydrothermal or oxalate routes only develops desirable electrical properties after grain growth in thermal processing.

Nanomaterials can be produced by a “top down” process by comminution of larger particles or by a “bottom up” process where particles are grown from a molecular template by combinations of gaseous, liquid or solid state processes as particles, planes or 3-dimensional structures. The first process is inexpensive but prone to contamination; the second process currently may involve expensive precursors.

The National Nanotechnology Initiative identifies nine “grand challenges”; materials, electronics, healthcare, environment, energy, microcraft, manufacturing, CBRE security, and instruments. Many of the non-electronics initiatives will develop sensors and other products that will require fabrication, packaging and electrical or optical interfaces fabricated using techniques used by the electronics industry. Some of these initiatives may develop materials potentially useful in electronic systems, such as advanced reactive powders used as functional fillers or minute lenses for optoelectronics systems. This obviously represents a business opportunity for our members.

In nanotechnology most of the applications are in the pre-commercial stage and will need development not only of the product but also modeling techniques and metrology. There is extreme diversity of potential applications but a commonality in fabrication techniques used, examples of which are thin film or plating deposition for layered structures and vapor, emulsion, or solution precipitation for powder structures.

Aspects of Nanotechnology relevant to NEMI

Nanotechnology will contribute a number of products and processes that are relevant to electronic processes. These range from the extremely long range and innovative to the short range and drop-in, including:

- Quantum computing using “peapod structures” based on carbon nanotubes (CNT) or Bose-Einstein atomic clusters; long term
- Transistors based on CNT or GMR layered structures; long term
- Plasma display technology based on CNT emittors; medium term.
- Advanced fillers that are reinforcing, thermally conductive, electrically conductive, TCE modifying for mold compounds, underfills, adhesives and board materials; short term
- Mixed Nano and MEMS sensor technology; medium term
- DNA strand self-assembly of electronic structures; long term

The commercialization of these products will depend on cost and performance when substituting for existing systems, and on the dynamics of new market creation. Obviously, the former is much easier to predict than the latter.

The NEMI Roadmap process will continue to monitor advances in these new technologies and materials, and to assess how these advances meet the R&D needs of the electronics industry. Appendix E highlights some of the needs from the 2002 Roadmap that might be addressed by nanotechnology.

Table 2: Potential Areas of Nanotechnology Impact

Fields in NNI	Desired commercial and military products enabled by nanotechnology
Nanoelectronics and Information Technology	Nano-structured microprocessor devices with orders of magnitude lower energy use and cost per gate, thereby improving the efficacy of computers by a factor of millions
	Communications systems with higher transmission frequencies and more efficient use of the optical spectrum to provide at least ten times greater bandwidth
	Small mass storage devices with capacities at multi-terabit levels, 1000 times better than today
	Integrated nano-sensor systems capable of collecting, processing, and communicating massive amounts of data with minimal size and power consumption
	Programmable, “smart” materials for multifunctional applications
Medicine and Health	Artificial, inorganic, and organic nano-scale materials cells to play roles in diagnostics (e.g., quantum dots in visualization), and also for use as active components
	Effective and less expensive health care using remote and in-vivo devices
	Hearing and vision aids, and other sensors that compensate for impaired human signal processing
Aeronautics and Space Exploration	Low-power, radiation-tolerant, high performance computers and nano-instrumentation for space applications
	Next generation avionics made possible by nano-structured sensors and nano-electronics
Environment and Energy	New, “green” processing technologies that minimize the generation of undesirable by-product effluents
	Efficient, small, light, cheap, long-lasting batteries and fuel cells for portable and consumer electronics
Biotechnology and Agriculture	Nano-array based testing technologies for DNA testing
National Security	Enhanced automation and robotics for all combat vehicles to offset reductions in military manpower, reduce risks to troops, and improve vehicle performance
	Higher performance (lighter weight, higher strength) military platforms with lower failure rates and reduced life-cycle costs
	Chemical/biological/nuclear sensing and improved instrumentation for casualty care
	Sensor systems for nuclear non-proliferation monitoring and management

Appendix A: R&D Needs Sections from 2002 NEMI Roadmap

This appendix reviews the R&D needs findings from the 2002 roadmap. The needs are described for each Technical Working Group in the following order:

- Board Assembly
- Connectors
- Energy Storage Systems
- Environmentally Conscious Electronics
- Final Assembly
- Interconnect Substrates - Ceramic
- Interconnect Substrates - Organic
- Mass Data Storage
- Modeling, Simulation and Design Tools
- Optoelectronics
- Packaging
- Passive Components
- Product Lifecycle Information Management
- RF Components
- Test, Inspection, and Measurements
- Thermal Management

Board Assembly

Technology Needs

The underfill process has provided faster flow times but challenges exist with reworkable and pre-applied underfill for standard SMT operations. Standards that address the quality and reliability of a site (once it is cleaned up in the rework process) are necessary. Collaboration between fluid formulators and re-work equipment suppliers will be needed for optimization of process efficiency.

Recommendations

The following are the recommendations for technology development for the electronics industry. The recommendations are placed in prioritized within each category.

Business Issues:

1. With the changing mix of manufacturing within North America, time to market will become a critical differentiator for companies.
2. Because of the level of integration between OEMs and EMS's, the industry needs to find mechanisms to safeguard intellectual property rights across many countries and cultures.
3. Assembly and component labeling standards for lead-free need to be developed to minimize long-term reliability issues.
4. Development of engineering and process development collaboration tools and standards will be necessary.
5. Adoption and enhancements to intelligent electronic data will be required.
6. To optimize the adoption of new board finishes and package technologies, a survey of the current state of the technology is needed. This adoption band will allow for appropriate allocation of R & D resources by equipment suppliers and assemblers.
7. To minimize the labor required to trouble-shoot components on the production lines, a notification process for component package changes needs to be created.

Equipment:

1. Adoption and enhancement of the tools to support highly flexible SMT lines will be needed.
2. Automation of optoelectronics assembly will become a differentiator for the North American electronics industry. This will require review of the component standards and development of packaging standards.
3. To reduce the MTBA for NPI, smart parameter algorithms need to be developed for machine parameters.

4. Integration and development of feed forward technologies to eliminate the requirement for strong technical competence by the operators and to decrease DPMO rates.
5. Development effort is needed to produce throughput and paste deposition performance (in data drive solder deposit methods) that are comparable to or better than stencil printing technology.
6. The proliferation of tools should be accelerated in order to optimize the entire manufacturing process.
7. Increased aqueous wash cleaning capability under high I/O and large components is necessary.

Materials:

1. Development of tests and standards to identify and control black pad on ENIG will be needed.
2. Increased process capability for lead-free products in the reflow process should be implemented through development of improved manufacturing materials.
3. Thorough study of the effects of assembly processes and materials on high frequency products should be undertaken.
4. Collaboration is needed between underfill fluid manufacturers and rework equipment suppliers to provide highly reliable, reworkable, underfill products.

Connectors

Key areas for connector development activities during the next 5 years include:

- High speed / high density backplane connectors (over 100 signal contact per inch, both differential and single ended signal applications)
- High speed copper cables (Infiniband, Fiber Channel, 10Gb Ethernet, etc)
- LGA sockets (focus on high I/O $\geq$ 1000 contacts on 1mm pitch)
- Parallel optical interconnections
- Higher performance memory sockets (card edge DIMM (dual inline memory module) sockets have high wear and low reliability and will eventually be replaced)

Time-based reference information for connector and cable technology roadmaps, as illustrated in this chapter, is considered problematic by some since most new connector developments are based on industry standard initiatives or specific customer requirements, not virgin R&D (research and development) developments by connector companies.

Core Technology Competencies (Source: APEX Connector Consultants)

Connector technology is bounded by certain core technologies that are at the heart of all major connector manufacturing enterprises. Most challenges, such as the aforementioned shift to electronic modeling, fall within this modern set of competencies:

- Metallurgy & Metal Forming
- Plating
- Contact Physics
- Materials & Molding
- Assembly & Packaging
- Mechanical & Electrical Design
- Design for Manufacturability & Assembly
- Global Logistics & EDI (electronic data interchange)

Understanding this provides clues to a connector technology roadmap's direction and what some of the possible outcomes are. Key customers should be acutely aware of these capabilities, and take them into consideration in their own roadmapping efforts. In fact, it is not uncommon for new variations of “old” technology to win out in a new design contest, as was the case with the inveterate PGA or Memory sockets used in most PCs today.

Energy Storage Systems

Recommendations

- Fuel cell systems, lithium-metal/SPE technology, and thin-film batteries have the potential to provide very high energy density and specific energy. These technologies are recommended for further development on an R&D level. Fuel cell systems that operate near ambient temperature are possible power sources for portable electronic devices. Appropriate technology to store fuel for portable applications needs to be identified and hybrid power system design is also a priority.
- An opportunity for North American manufacturing to regain significant participation in the market. Disruptive technology (such as fuel cells) and overcoming substantive technical hurdles (e.g., developing batteries for electric/hybrid vehicles) offer a window of opportunity. In order to ensure success, North American manufacturers and governments must be willing to invest with a long-term perspective
- The mechanism for cooperation between industries and among researchers working on advanced battery technologies must be strengthened. Companies in Japan, Taiwan, Korea, and Southeast Asia are making huge investments in a global electronics development effort, and the effort is increasingly being extended to the power sources for these products. Cooperation between OEMs and battery suppliers is needed to focus on the right technology and to find a way to deploy it in a timely manner. Cooperation in the battery and chemical industries is needed to assure availability of new high-energy materials for commercial production.

Environmentally Conscious Electronics

Technology Needs Overview

Continued changes in the environmental characteristics of electrical and electronic products will require the development and implementation of new technologies to improve energy efficiency, eliminate hazardous or potentially harmful substances, and increase both the reusability and the recyclability of products. Most importantly, efficient, standardized methods for data exchange of environmental metrics and attributes must be developed and implemented. These metrics should be synergistic with Environmental Management System (EMS) methodologies and ultimately linked to the concept of environmental sustainability. Additionally, new information technology systems will be needed to assist product designers with selection of materials and components with reduced environmental impacts. There is a significant need to develop and standardize tools and definitions for Design for Environment (DfE) and Life Cycle Assessment (LCA).

Cost

One of the strongest drivers for any action within industry is cost. However, in order to use cost as an environmental driver, that cost must be accurately measured. Many companies either don't have a measure of their environmental costs or have an inaccurate (and usually underestimated) one. There is a strong effort within the printed wiring board and assembly sector, led by the IPC, to improve the understanding of environmental costs. This effort has been aided in part by the EPA Design for the Environment project, which developed an initial survey on environmental operations costs including pollution prevention. This effort was similar to an earlier effort by the AESF (American Electroplaters and Surface Finishers Society) to examine pollution prevention costs in the plating industry. Further effort is needed by industry to quantify the total cost impact of environmental alternatives.

Alternatives to Materials of Concern

While most of the materials used in electrical and electronic products are completely safe for users of the products, some materials may be hazardous in the manufacturing process or contribute to environmental problems at the end of product life. In most cases, these materials are used in electronic products due to unique functional requirements. Cost-effective functional equivalents are needed for the following material applications:

- Pb in solders, glasses, plastic stabilizers, and ceramics
- Cd in plastic additives and coatings
- Cr VI in surface finishes
- Hg in lamps and plastic stabilizers
- Beryllia ceramics and beryllium in alloys
- Phthalate softeners for plastics
- PBB and PBDE in plastics

Energy Efficiency

Concerns over the possibility of global warming due to the burning of fossil fuels will result in increased demand for energy efficient electrical and electronic products. An essential goal of designing more energy efficient products is the selection and use of components and devices with lower power requirements. New advances will be needed which facilitate the development of faster devices with even lower power requirements. However, the reduction in power alone will not be sufficient to offset increased functionality requirements and the resulting increasing energy requirements for electronic products in the next decade. The increased use of battery-powered devices places increased emphasis on the efficiency of the charging system. To meet the demand for energy efficient products, electronic product manufacturers will need to implement new power management techniques to ensure that energy is not wasted while products are idle or unused. The implementation of effective power management for electronic products will require cooperation among component manufacturers, system manufacturers, and operating systems suppliers. While standards have already begun to develop for management of important system components such as storage devices and monitors, additional power management standards will be required.

End-of-Life: Product Recyclability

Products containing restricted or banned materials are more costly and difficult to recycle because of regional, restrictive legislation. Thus, many OEMs and industrial customers are working to eliminate these materials through Design for Environment (DfE) to reduce end-of-life and total life cycle costs. This trend will accelerate as jurisdictions pass “take-back” legislation to reduce the burden on landfills. In order to avoid landfill use for huge numbers of products, it will be necessary to develop a cost-effective infrastructure for reuse and recycling of electronic equipment. While some metals and components commonly found in electronic products can be recovered, plastic materials present special challenges. Currently there is no viable recycling process for the epoxy-glass content of PWBs (Printed Wiring Boards) except energy recovery and only limited recovery of plastics used in enclosures. Alternative technologies for recycling electronics are being prototyped in a number of countries. Promising processes need to be commercialized. Several new technologies are being developed to facilitate the recycling of plastics. First, automated sorting processes are required to facilitate plastics identification and separation. New processes are needed to clean the materials and remove paints and labels in an economical manner. New secondary and tertiary uses must be identified for plastics where quality and or cost considerations preclude reuse in electrical and electronic products.

Tools

In order to understand the complex decision and tradeoff process used in the design of products for minimum environmental burden, new life cycle assessment and Design for Environment (DfE) tools will be required. These environmental assessment tools will need to be integrated into the mechanical design tools used by designers to develop products once their validity has been scientifically demonstrated. These tools should address the “triple bottom line” including cost-benefit analysis. Much R&D is still required before LCA can become a reliable and practical methodology for making design decisions, let alone being used as an approach to policy decisions or regulations. For example, is it better to reduce the energy use of a laptop by using Hg containing back light bulbs or to eliminate the Hg to reduce the eco-toxicity?

Information Management

The final area where new technology will be required in order to improve the environmental characteristics of electronic products is in information management tools. Of primary importance is the development of standards and requirements for collection, documentation, and transmittal of information about the material content of components, assemblies, and systems. Not only is this information needed to effectively and safely dispose of products at end-of-life; it is required by systems manufacturers and their suppliers in order to respond to the growing number of environmental inquiries related to their products. EICTA, EIA, and the Japanese Green Procurement Group of JIETA are working to standardize the list of materials that will be reported. Along with information on the content of components, assemblies, and products, it will be necessary to develop standardized toxicological and environmental profiles for materials and processes used in electronic products, along with their alternatives.

An industry-standard, information management system to exchange environmental information is needed today. The automotive industry has been addressing this issue for several years as they respond to legislation concerning material bans and recycling targets. Without the effort to first standardize the information requirement at the OEM stage, the Tier 1 and subsequent suppliers are faced with a plethora of forms and databases from their customers. These requests for information place an enormous burden on companies as they pass requirements down the supply chain, quantify the material composition and associated substances of their products, and transmit the data to the customers in a variety of desired formats.

Final Assembly

Technology Needs

The cost of final assembly needs to be systematically reduced. From Table 4 we can see that the cost of process modules, tooling, and integration for an application normally exceeds the cost of the base platform. Improvements are needed in the following areas in order to achieve the cost targets defined in this roadmap.

Design for Automated Assembly

This is an area in which the U.S. and Europe are at a disadvantage relative to Japan. This is due to our inability to make appropriate compromises between design functionality, component manufacturability (including manufacturing process and tooling), and assembly process complexity. While co-location and simultaneous engineering of product and process improves the odds of success, a variety of tools is needed to bridge the experience gap. Furthermore, DFA/DFM needs to be emphasized in engineering curricula.

Design for Disassembly

The consumer electronics industry has been actively working to prepare for widespread product take-back legislation. This legislation encourages the development of Design for Disassembly guidelines and methodologies as well as technology for product disassembly and content classification. This will drive flexibility, as a mix of products will need to be recognized and accommodated. This is also likely to drive increased standardization in the product design process.

Standard Base Platforms

One of the key components of cost reduction is reducing the costs of application development and deployment, including both engineering and integration costs. The reuse of standard process modules and existing designs is one way to reduce these costs. However, reuse does not occur in a vacuum; it occurs in the context of a framework or architecture. A standard base platform for a cell would provide an architecture for the reuse of mechanical, electrical, and software components. This platform would facilitate the reuse of standard process modules and the development of standard process modules by third-party suppliers.

Systems Integration

Most of the equipment suppliers in final assembly and packaging have implemented information systems using proprietary specifications. Some OEMs and EMSs request SECS/GEM (Semiconductor Equipment Communication Standard/Generic Equipment Model) interfaces that are not always suitable; e.g. in the case of equipment with moderate functionality. The final assembly and packaging area is calling for an explicit and scalable solution. CAMX (+) (Computer Aided Manufacturing) standards developed for PWB manufacturing don't cover the needs of final assembly and packaging where new levels of abstraction are needed (e.g. pallet based transportation with branching routes). Development of an IPC-2546 section of standards dedicated to final assembly and packaging has started and is expected to improve the information flow, integration, and plug and assemble capability. This would mean lower integration costs. In addition, end users are able to select the best-in-class machines and integrate them into multi-vendor systems. Finally, the use of a standard messaging format (Extensible Markup Language, XML) provides a homogeneous environment from equipment through enterprise to B2B (business to business).

Standard Process Modules

Standard Process Modules (SPMs) are plug-and-play modules such as those for screw driving, pick and place, vision inspection, etc. for use in standard cells. These modules have well-defined mechanical, electrical, and software interfaces, which enable them to be quickly added to or removed from the cell in response to application requirements. Standard process modules would include mounting hardware, cabling, and software drivers, allowing them to be installed on a cell much like a standard printer can be installed on a desktop PC. Standard process modules also lend themselves to the application of engineering analysis, simulation, and optimization techniques.

Flexible Parts (Components) Feeding

Another major challenge is the cost-effective flexible feeding of parts. Most commonly used bulk part feeders require large quantities of parts for the final revision, in order to test and refine feeding performance. The refinement process typically involves more art than science.

Software Development Tools

Most cell controllers use proprietary, vendor-specific operating systems and development tools. In order to promote reuse in the software domain, state of the art programming environments are necessary. These environments allow standard software components to be created for User Interface, Cycle Sequencing, Error Handling, Event Logging, etc.

Interconnect Substrates - Ceramic

Technology Needs

- Finer Lines / Smaller Vias: Combine photo patterning with tape and paste to allow patterning of line pitches below 100 µm and via pitches below 150 µm.
- Embedded Passive Components: Adopt thick film resistor and hi-K capacitor technology for compatibility with LTCC Tapes. For inductors, apply photo patterning to create high-density spiral patterns.
- Lower K Dielectric: Materials are needed with lower dielectric constant from current levels, to further improve the performance of high-speed digital signal applications.
- Process: Advanced via formation techniques including mechanical, laser, and photo via tool sets will provide the means to allow vias to achieve smaller sizes. For thick film printing, advances are needed in mask tolerances and controls, thick film paste rheology control, optical alignment of mask to pattern, and improved thick film printing, mask release controls. To achieve finer line widths (<25-50 µm), metal mask technology is required to extend the tolerance control beyond what is currently achievable using conventional wire mesh (emulsion) screens. Alignment of multi layers using optical techniques, along with improved dimensional control through better shrinkage control can provide the desired high interconnection and wiring density needed in future ceramic applications. Developers of AOI systems are keeping pace with the industry trend of smaller circuits with more complex patterns and features. Faster image processing and improved imaging techniques are a matter of course. However, there is a growing demand for AOI systems that offer seamless integration. This integration requires innovative sheet handling techniques combined with the networking of all process equipment. This seamless solution will provide manufactures with complete process control, reduce production costs, and enable the highest possible yields.
- General: In addition, a stable N_2 fired resistor system and improved dielectric compositions are needed to expand the potential of pure copper metallization on ceramic capability. Larger substrates are needed and have been developed. These must be a minimum of 225 in^2 with improved dimensional and mechanical feature tolerances. Also, to increase the usefulness of these technologies, large substrate machining capabilities are needed.

Interconnect Substrates - Organic

Technology Needs

Technology needs are divided into two major segments: Research Needs and Development Needs. Each has their challenges and opportunities:

Research Needs

- Resistless processes or permanent resists
- Laser direct imaging (writes)
- High-performance resins
- Integral materials for resistors/capacitors/inductors
- Self reinforced materials
- Liquid crystal polymer.
- New testing techniques and new cost effective electrical test methods
- Boards without surface finishes
- Improved dimensional stability materials

Development Needs

- Microvia technology improvement
- Microvia metallization
- Multiple microvia layers
- Continuous cycle time reduction for quick turn boards
- Improved design tools for emerging technologies

Mass Data Storage

Technology Needs: Research, Development, Implementation

For a given set of storage components (heads, media, spindles, tape drive paths, etc.), the more data on a given medium, the lower the overall cost per megabyte. Head and media work continues at many laboratories, with progress being made. Much of the advanced work done in media and heads is of basic science content, and support has to be found for this work. Due to business demands, companies manufacturing magnetic storage products may not support long-range work needed to ensure future solutions in all areas. Universities are a natural place for the work to be conducted, and the emergence of seven centers at major North American universities (Carnegie Mellon University, University of California San Diego, University of California Berkeley, University of Minnesota, Santa Clara University, University of Alabama, and Stanford University) has helped. In addition, the guidance of industry-wide programs under the International Storage Industry Consortium (INSIC) can provide a key role in these longer - term "main line" storage programs, and has fostered collaboration throughout the industry. This collaboration can also be enabled by Advanced Technology Program (ATP) funding and new metrology technologies being developed by the National Institute of Standards and Technology (NIST).

Research areas needing development to support the growth of magnetic recording include perpendicular and patterned recording media, tunneling magnetoresistive heads (TMR), heat assisted magnetic recording (HAMR), recording channel and preamplifier design, dual actuator servo systems, and advanced motor and actuator design.

With magnetic rigid disk drive areal densities exploding at a 100% annual growth rate (densities doubling every year) track pitches are fast exceeding sub-micrometer dimensions. Locating data and staying centered on the sub-micrometer tracks during reading and writing, while the medium moves past the transducer at almost 100 miles (160 km) per hour, is a huge engineering challenge. Taking advantage of recent advances in materials and processing, the disk drive industry is beginning to employ aspects of micro-electromechanical systems (MEMS) to increase the servo system bandwidth to overcome motor bearing non-repeatable runout and other eccentricities. This enables narrower track widths and faster data transfer rates. The disk drive industry is staging the introduction of these devices. The first application may involve macroscopic piezoelectric devices that move the entire head slider (the magnetic transducers together with the mechanical air bearing) relative to the flexure. This approach provides a modest increase in the servo bandwidth.

Second and third generation devices, due to be shipped in two to four years, will extend silicon micro machining and incorporate fashioning micromotors or microactuators directly on the slider. Microfine positioning of the transducer will then be accomplished through moving the thin film transducers only. This virtually massless motion will significantly broaden the servo system's bandwidth. With the increased bandwidth, data tracks can be narrowed and spindle speeds increased, raising data transfer rates. These gains are essential for recording system growth and continued rapid progression. Enhancements to magnetic tape storage, where track following is aggravated by flexible media, is also enabled with this technology. It is expected that tape data storage will share in the servoing improvements that MEMS can provide.

Some unconventional approaches to data storage are also enabled by MEMS. Magnetic data storage systems using non-rotating and non-streaming media (but not all solid state, as with MRAM) still require relative motion of a transducer over the medium. Probes and arrays of transducers have been proposed and some are under development for the reading and writing of non-rotating media. Various MEMS approaches include moving each transducer individually, and moving an entire block or array of transducers simultaneously. MEMS is also enabling other storage technologies such as holographic optical storage. Advanced micro-machined light modulators have been developed using these new materials and processing techniques.

The optical mass data storage area is continuing to grow in terms of areal data density and data transfer rate and shrink in terms of cost and equipment size. In order to continue to have an opportunity to participate in this market, North American manufacturers need to continue to develop technology consistent with these market directions. In the current configuration of optical storage devices, areal data density is a function of wavelength of the recording beam and objective lens numerical aperture. This implies that technologies needed for improvement in this area are semiconductor lasers capable of operating at shorter wavelengths, and optical lens configurations with higher numerical apertures. There are also approaches with media that allow a fixed size spot to read or write denser data. These techniques include land/groove recording, multi-level recording, magneto-optic super-resolution, and improved data detection techniques such as PRML. Improved areal density techniques being investigated by some companies include near-field and optical flying head technologies. Development of high-volume, low-cost manufacturing approaches will be key to the success of these new technologies. Increasing the per channel data transfer rate will require: higher speed digital encode/decode channels, higher power semiconductor lasers, higher speed spindles, improved recording materials and/or increases in the in-track data density. The overall device data transfer rate can also be increased by use of multiple recording heads and/or multiple data recording surfaces. The higher data rates generate a strong need for improved circuit board design tools that incorporate the RF design factors and transmission line layout into the process. This will become increasingly important to maintain satisfactory signal quality and robust data transfer performance in future products. Decreasing the cost will require reduction in parts count, materials cost, and more efficient assembly and test processes. This will require simplification of the mechanical elements of the drives as well as greater electronics integration.

Decreasing device size will require minimizing dimensions of mechanical and optical elements as well as increasing the electronic packaging density. Decreasing device size also increases the difficulty of heat removal and may necessitate reduced power dissipation for equivalent performance.

Modeling, Simulation, and Design Tools

Emerging Areas for Electronics Packaging

There are several new areas in which electronics packaging promises to play a major role. Table 8 summarizes the needs in these areas up to the years 2007. These are the MEMS, nano-scale, Spintronics and the Opto-PWB areas. Table 8 summarizes the key simulation issues in each of these areas as well as the critical year is highlighted. These areas are in the nascent research stages and there seems to be enough time for research, with the only exception being the MEMS devices proliferation in the automotive sector by 2005 which needs urgent attention.

Table 3: Projected Development and Research Needs For Simulations in Emerging Areas

Emerging Simulation Area	**Needs by 2003 to 2007**	**Comments**
Opto-PWB	Robust tools to predict and optimize optical loss Predictability of the effect of thermal, moisture, stresses on optical loss Integration of optics and electronics in PWBs - design methodology Simulations (thermal and mechanical) for optimizing hybrid lamination schemes for electrical and optical needs	Limited wave propagation tools available Critical in 2005-2007
MEMS	Multi-phase flows simulations, bioMEMS Multi-physics simulations: (e.g. Joule heating in sub 50 nm interconnects, electro-chemical phenomena in bio-MEMS devices) Multi-scale simulations from sub 50 nm to mm (similar issue to nano-scale methodology) Methodology to predict failure of MEMS devices - e.g. delamination, cracking - surface & material science Analog & digital design	High volume production is a challenge - many custom processes different from usual Si foundry Lack of standards New experimental techniques may also be needed to verify the modeling algorithms. Very accurate displacement measurements will be required. New failure modes and mechanisms will need to be identified. Limited commercial software packages available, criticality in 2005
Spintronics	New materials optimized for spintronics - electrical, delamination, moisture Modeling & simulation of spin as electrons move through different materials, spin relaxation modeling	Exploit spin for storing data 10.6 B Flash memory market, 35 B RAM market Exploit for Logic? Wafer-package convergence Long-term/research phase - keep a watch; critical 2005 - 2010
Nano-Scale Modeling & Simulations	Thermo-mechanical models for nano-scale Experimental tools capable of measuring electrical & thermal and mechanics phenomena/material properties at smaller scales Scale dependent algorithms will be needed - ability to shift scales	Drivers: Wafer-package convergence Device/package circuitry moving to smaller scales: < 65 nm in 2007 Advanced materials e.g. TIM (Thermal Interface Materials Issue: How is the property and behavior different from bulk behavior/macro-scale? Critical in 2007

Optoelectronics

Technology Requirements

Standards

- Packaging represents one of the highest costs of current O/E components and also represents a major cost to using these components in higher assemblies. New packaging standards must be developed to address changes in reliability, scope and usability.
- Reliability standards are well established for the telecommunications backbone networks. New standards should be established for other applications including datacom and premise applications.
- Interoperability standards need to be established to allow for the mixing and matching of hardware to achieve more competition and better production scales. Engineered links that guarantee optical performance end to end to interoperable standards would also significantly reduce the CAPEX and OPEX costs to service providers.
- Testing needs to be standardized so lower cost test equipment can be developed for use in both manufacturing and in the field.
- Improved transport standards to support data protocols.

Automation

- Improved subcomponents and materials that lead toward automation will be key to supporting the higher volumes expected at the edge of the network. This includes self-aligning structures and structures that can be assembled without concern regarding changing alignments. Also materials that are recognized and expected to meet specific reliability and performance requirements for various market segments need to be certified for specific application so that both risk and costs are reduced.
- Assembly processes and equipment that support integrating electronics and optics into single packages will play a role.
- Improved fiber management or elimination of fiber where possible will allow for conventional electronic processing of modules into board level products.
- Design tools that support specific manufacturing processes and also support integration of analysis will speed products to market and reduce development costs.

Integration

- Technologies must be developed that support effective hybrid integration of components into lower cost, smaller, higher functioning subsystems.
- A combination of materials and fabrication research is needed to support the development of monolithically integrated optics and electronics to take advantage of the electronics infrastructure.
- Technology development is needed in areas such `optical solders' and board level wave-guides to enable more complex and higher density board level products.
- More intelligent network management will facilitate taking advantage of transport capability and services and will improve network utilization.

Device Technology

- Development should continue in areas that promise lower cost optical components such as SOAs, VCSELs, and semiconductor switch products.
- A system wide view of thermal management should be established to assist reduction of power consumption and to keep the cost of optical components within operating ranges. Improvements can be made by developing more stable optical materials and designs, using heat pipes and other methods to remove heat from high-density components and board level products, and the use of more efficient cooler technology.
- More advanced development of photonic crystal or other technologies that can promise to put photonics on a size reduction roadmap such as that enjoyed by electronics is needed.

Packaging

The most difficult challenges facing the assembly and packaging industry are presented in Table 4 below. These challenges are intended to provide a mechanism to allow the research community to focus resources in the areas of greatest need.

Table 4: Packaging Challenges through 2007

Difficult Challenges (Through 2007)	**Summary of Issues**
Improved organic substrates	Tg (Glass Transition Temp.) compatible with lead-free solder processing
	Increased wireability at low cost, substrates are a barrier to flip chip adoption
	Improved impedance control and lower dielectric loss to support higher frequency applications
	Improved planarity and low warpage at higher process temperatures
	Low moisture absorption
	Low-cost embedded passives
Improved underfills for flip chip on organic substrates	Improve flow, fast dispense/cure, better interface adhesion, lower moisture absorption
	Higher operating range for automotive and Pb free soldering in liquid dispense underfills
	Improved adhesion, small filler size, and improved flow for mold based underfills
Coordinated design tools & simulators to address chip, package, and substrate co-design	Chip, package, and system level co-design tools
	Educational programs required to train engineers in co-design technologies
	Faster analysis tools for integrated thermal mechanical analysis
	Higher accuracy, faster electrical simulation capability for high frequency design
Impact of Cu/low κ (dielectric constant) on packaging	Direct wirebond and bump to Cu (Copper)
	Bump & underfill technology to assure low κ dielectric integrity
	Improved Mechanical strength of dielectrics
	Interfacial adhesion
Pb (lead), Sb (antimony), and Halogen free packaging material	Lower cost materials and processes to meet new requirements, including higher reflow temperatures.
Difficult Challenges (Beyond 2007)	
Package cost which may greatly exceed die cost	Reliability under thermal cycling (stress and moisture)
	Research investments required for packaging cost reduction are decreasing
Small, high pad count	Array I/O pitches below 80 microns
High Frequency die	Substrate wiring density to support >20 lines/mm
	Lower loss dielectrics
	Skin effect above 10Ghz

Close gaps between substrate technology and the chip	Interconnect density scaled to silicon (silicon I/O density increasing faster than the printed circuit
System level design capability to integrated chips,	Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliabiity, and cost of complex systems very difficult.
Passive components and substrates	Complex standards for information types and management of information quality along with a structure for moving this information will be required.

CTE - Coefficent of thermal expansion, ** UBM - Under bump metallurgy, †-EMI-Electromagnetic interference, ‡ EDA-Electronic design automation

The following narratives provide background information on six critical research needs.

Critical Issues

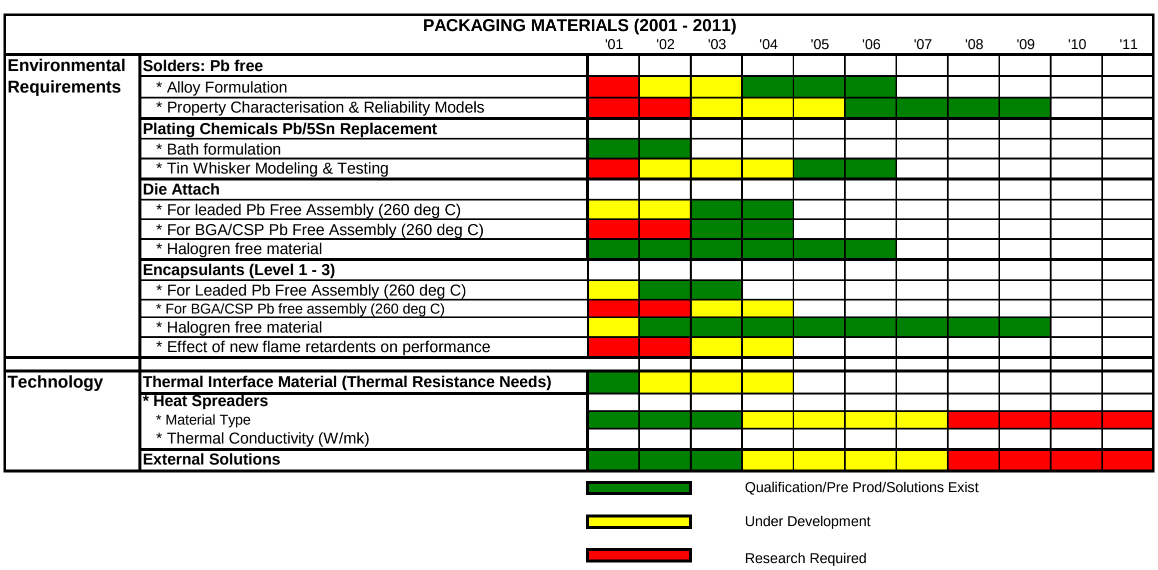
Package Design Requirements

With the evolution of System In Package (SIP) based products, the industry has started to develop integrated chip and package design tools for high frequency and mixed signal designs. This capability will need to be extended to enable concurrent chip, package, and system design. The design complexity (chip-to-module and chip/module-to-board) and scope are continuously increasing, while the market intensifies the demand for design cycle time reduction and high design confidence. Physical, electrical, thermal, mechanical, assembly, and manufacturability considerations, in addition to cost and availability, confront the package designer. The package design process requires continuous improvements in design and analysis tools. The tools for layout, wiring, electrical, mechanical, and thermal design tasks must enhance usability and minimize interface incompatibilities if design cycle reductions are to be realized. The goal is an integrated design system. The scope of this integrated design system must include or be coordinated with chip design so that efficient chip/package co-design is feasible. Ideally, it should be linked to the system design so as to incorporate those requirements and tradeoffs.

Packaging Materials Requirements

Dramatic improvements in materials properties will be necessary to address high frequency, higher power density, and increased mechanical stress demands that will be required to support advances expected in 2005 through 2016. Materials such as encapsulents (including mold compounds) and solder die attach are expected to be especially sensitive to environmental concerns. For example, there is presently no known drop-in replacement for Pb-based solder die attach. Additionally, performance indicators like dielectric constant, dielectric loss and thermal conductivity will become more important in meeting higher frequency and higher power demands. There is an urgent need for packaging material databases, characterization methodology for materials, and materials interface properties. Packaging materials databases are needed for modeling and simulation of electrical, thermal, and reliability performance.

Table 5: Package Materials



MEMs requirements

MEMS technology has broadly expanded in the last decade to become the standard for many automotive, medical, telecommunications, and consumer electronics applications and the predicted market growth for MEMS technology is very high. One of the major bottlenecks for the continued growth of MEMS products has been packaging technology.

Like standard semiconductor devices, MEMS devices need environmental protection, electrical signal integrity, mechanical support, and thermal management. However, in addition, MEMS may require packaging that provides access to chemical or biological environments they interact with. Many of the MEMS applications also demand inert/vacuum inside the package. For example, pressure sensors that are media compatible for a disposable blood pressure application are not media compatible for a 10-year automotive application. As a result even though the functionality of two MEMS could be the same, the differences in environment require quite different package designs. To effectively reduce cost, improve manufacturability, and improve reliability, standardized technologies need to be developed which can handle this broad range of requirements. MEMS do not require high pin counts or very fine pad pitches for interconnect. Some single chip ceramic, molded, chip scale, and wafer level packaging technologies have been used successfully to address some of these applications' requirements. However MEMS multichip packages and 3D packaging solutions are still under development.

To meet product performance requirements, MEMS devices (and packaging designers) must consider the interface of structural elements, signal processing and power elements, signal and energy changing elements, material technology, harsh media compatibility, test equipment processes and standards, and packaging techniques and processes. While many of these issues are common in semiconductor packaging, some are unique to MEMS. CAD systems' package design standards and methodologies, packaging assembly attributes, reliability standards, and assessment and interfaces of micro and macro packaging attributes need to be developed to handle these unique design requirements.

RF and Mixed-signal Requirements

The packaging challenges in this area will become increasingly important as low-cost mobile and high bandwidth products expand across all market segments. The increasing performance of silicon, SiGe (Silicon-Germanium) and GaAs (Gallium-Arsenide) devices, coupled with dramatic device cost reductions, have establish the need for very low cost, high performance packaging. The primary approach to date has been to focus on extending the performance of low cost wirebond packages through careful design optimization. However this approach will not support continued cost reductions and performance improvements in the long term. In the RF product area, frequency will shift up to the 5 GHz range, which will require improved dielectric loss, tighter control of parasitic variability due to process variations, and more precise electrical simulation capability. Flip chip attachment to package and embedded passives on the package will be key enabling technologies to package level performance. Low inductance and high-density packages like FBGA/CSP will enable designers to use lower cost partitioning solutions than the traditional ceramic modules.

Integrated modeling and simulation tools are required to drive down design cycle time to acceptable levels. Performance, physical size, and cost driven integration will continue to arrive at a single chip radio that combines memory, processor, and mixed-signal functions, as discussed above. Fast design cycle time and accurate simulation at both the chip and package levels are enablers of this integration. High-speed test and higher levels of functional test at the package level also become development challenges. Micro-electromechanical Systems (MEMS) will be used in the fabrication of filters, switches, oscillators, and other components in the next 2-4 years. They offer the benefit of small size, low insertion loss, low power consumption, integration with ICs, and the potential of low cost with batch fabrication. Reliability, potential temperature sensitivity, and hermetic/vacuum packaging of MEMS devices are key development challenges.

Multi-chip Packages/Multi-chip Modules/System in a Package

Beginning in 1999 and driven by mobile phone applications, a shift has been occurring in multichip packaging propelling the SiP (System in Package) into becoming the fasting growing area of packaging (due to its associated system integration benefits). The reason for this shift is that the SiP has enabled OEMs to maintain their size / weight reduction roadmaps while integrating more features and functions through system package integration. This integration challenge may be best realized through cooperation between OEMs, their semiconductor device suppliers and microelectronic manufacturing service suppliers. The OEMs in these mobile phone applications have shorter product life cycles and have come to the realization that designing new products is easier and more cost effective when you do not have to reinvent each detail from scratch. The new definition of SiP could be as simple as adding passive components to a single chip package, or as complex as having multi-chips and or stacked chips in a single package with all the passive components included to provide a subsystem functional block. The SiP can be manufactured using Ceramic, Leadframe, Organic Laminate, or even tape based substrates. The passive components can be embedded as part of the substrate construction or be soldered or epoxy attached on the substrate surface.

Die interconnect can be accomplished by wire bonding, flip chip (soldered or epoxy), or TAB (Tape Automated Bonding) to the SiP substrate, or die to die. The final package configuration can take the shape of a conventional Ceramic Style Package, Ball Grid Array, Land Grid Array, or Lead Frame based package or may be a custom module. The resulting SiP utilizes die to die interconnection and high density substrate technologies to handle the higher wiring density requirements at the package level thereby reducing the cost, wiring and I/O densities required at the mother board and system level.

Since SiPs were first adopted in high volume handheld and wireless applications, their resulting low cost infrastructure (through the utilization of proven packaging platform technologies in high volume manufacturing lines) is enabling new SiP configurations to be customized for a broad range of new applications. Any application that utilizes chip sets or embedded or large memory blocks (with high interconnect density requirements) should evaluate SiP for their cost / performance optimization needs. The SiP packaging concept can be considered as the fourth wave of packaging innovation and will remain important for the following reasons:

- Using SiP, different die technologies such as GaAs, GeSi, or Si and die functions such as logic, memory, RF, analog, or digital can be assembled in the same package to achieve specific thermal, electrical, and mechanical performance requirements.
- Dissimilar die geometrys can be cost effectively integrated from sub-micron of 0.10-0.13 to micron in the same package. The latest die technology can be used for each die function, thereby reducing cost and increasing performance.
- Other technologies such as MEMS , optical, or vision components may be included in the same SiP package.
- Various interconnection technologies such as wire bond, flip-chip, or tab can be used to connect to the package as well as to each other.
- In addition to passive components, antennas, filters, heat sinks, resonators, connectors, and shields can be included in the same package.
- Revisions or upgrades to OEMs products are easily accomplished by using the latest die functions, therefore reducing the cycle time for those changes.

As the ability of the semiconductor sector increases to build true Systems on a Chip (SoC), not all the different components that need to complete a system can be cost effectively integrated on silicon. The SiP would then take on the role of incorporating the other non-silicon components into the package with the SoC device. The SiP will continue to become more complex and cost effective as new applications emerge. The final factor in favor of the SiP is the short cycle time it takes to create a new SiP or a modification of a present design. The time from design and characterization to manufacturing can be as short as 3-4 months, whereas design of an SoC would take much longer. This is why the SiP is playing, and will continue to play, a critical role in component packaging and system integration.

The SiP category does require new metrics for measuring cost-effectiveness. The cost per pin paradigm does not apply well to SiP and multichip package applications because the SiP greatly reduces the number of second level connections through die to die interconnection within the package. In addition, the area and wiring density reductions associated with SiP provide system and motherboard cost reductions while enhancing reliability and performance. Both cost per area and total cost of ownership perspectives are required to fully appreciate the system integration cost and performance benefits delivered by SiP solutions. For instance, silicon efficiency is a new metric to measure the area effectiveness of bare die (wafer level packaging) vs. multichip and 3D packaging solutions. Bare die or WLP (wafer level packaging) achieve 100 % Si efficiency (where the die size and package sizes are equal) whereas emerging 3D (stacked die) packages are delivering over 200% Si efficiency using the previous measurement methods.

The SiP infrastructure will be facing the following challenges as it continues to grow:

- Acquiring sufficient and effective design tools
- Establishing modeling tools for both thermal and electrical aspects
- Encouraging an increase in cooperation between the manufacturer, semiconductor device suppliers and the OEMs

Modeling and Simulation

The ITRS Assembly and Packaging TWG has identified chip-package, co-design as one of the key crosscut challenges for the 2001 ITRS. This challenge specifies the need for modeling and simulation of mechanical, thermal, and electrical performance of the entire chip, package, and associated heat removal structures as a combined system. This capability is critically needed to insure cost effective and timely assembly and packaging solutions for devices employing new generations of Cu-low k metallization and high power, low voltage (SoC) System on a Chip structures.

The modeling and simulation needs in assembly and packaging, as in many other technology areas, are becoming much more stringent because of the larger number of parameters that must be included and the increasing impact of specific chip features on package performance, and vice versa. For example, the change to interconnects with low k dielectrics, low mechanical strength, and low thermal conductivity has placed much more emphasis on combined electrical and thermal modeling of the package and chip. Lower voltages and higher currents have significantly increased the need for chip-package, co-design to minimize the effects of high current transients on very low level signal lines. To address these critical requirements, the short term modeling and simulation capability needed requires the ability to link the simulation of macroscopic thermal and mechanical performance of packages with the microscopic electrical performance and thermal generation sources on-chip with both time and spatial resolution. The features needed range from high-level predictions of package high frequency performance and reliability for product engineering use, to detailed prediction of temperatures and mechanical stress at specific times and locations for device and package design tasks. Modeling and simulation are required to provide accurate predictions in order to eliminate the need for running extensive, costly experiments. These requirements run from predictive capability within experimental error for relatively mature technology approaches, to accurate identification of restricted experimental parameter ranges for new approaches.

It is anticipated that the short-term modeling and simulation needs of assembly and packaging will be addressed by non-optimally combining available capabilities or by evolutionary extensions of these capabilities. In the longer term, it is desired that a more complete systems approach be provided. In particular, assembly and packaging needs from modeling and simulation are:

- Tools for assembly and packaging performance prediction (including reliability and high frequency effects), especially for complex structures with hierarchical capability to trade off speed and accuracy to meet specific applications.
- Tools and methodology to connect product and process design in an integrated flow to meet target specifications or identify deficiencies.
- Materials modeling capability to predict structure as well as physical and electrical performance from atomic and molecular information.

Assembly and packaging technologies must meet very demanding requirements in the areas of performance, power, junction temperature, and package geometry. Therefore, advanced modeling tools are needed that cover electrical, thermal, and mechanical aspects. These phenomena can no longer be described independently. Major advances are needed in the individual tools (and in their integration) to achieve a self-consistent solutions and to integrate or coordinate with chip design software. To move to 3GHz chip-to-board speeds, the modeling of electrical signal propagation, noise, and radiation needs to be improved substantially both in computational (run time) and input efficiency, and in the ability to address realistic complexity, configurations, and conductor density. Mechanical stresses need to be coupled between chip and package level. The introduction of low * dielectrics (with low thermal conductivity) will increase the need for accurate thermal simulation, which needs to be compatible with electrical behavior, given the higher power dissipation levels.

Modeling the electrical behavior of systems of chips packaged individually or collectively in single or multi-chip packages is pushing the practical limits of what can be done in a cost and time effective manner, even at existing clock frequencies. Extension of modeling and simulation techniques to higher clock frequencies and higher densities will require significant research to provide useful design capability. Other reduction techniques, either time-domain or frequency-domain, will be required to achieve useable run times. Full-wave simulation tools will be required in order to deal with some complex structures, and they must be computationally efficient. Integration or interfacing of package- and chip-level design and simulation systems will be a necessity as the options for interconnect placement (on-chip or on-substrate) occur. Integrated chip, electrical (architecture), mechanical, thermal, and cost modeling tools will be useful for integrated design and manufacturing teams, with potential for cycle time reduction.

The industry continues to increase power dissipation, junction temperature, and reliability expectations that push the cooling and mechanical strength limits of electronic products. More comprehensive thermal and mechanical modeling tools fully supported by "real life" materials data and correlated with physical measurements are needed. Examples include fluid and solid models for air flow characteristics, stress predictions in accelerated tests and power cycles, micro-models for interface fracture behavior, and macro structure models for package dynamics behavior including vibration and mechanical shock. These model methods are also being applied to manufacturing and assembly processes such as adhesive/underfill flow or BGA rework. Better experimental capability for measurement of *in situ* properties, location, and characterization of defects and failures are needed. Key is development of *in situ* model mechanism elucidation and validation tools such as micro-Moiré, Nan indentation techniques, and interface fracture toughness techniques.

Passive Components

There are many technological needs in integrated passive development. Five of the most important are listed below:

- Determine the Amount and Distribution of Capacitance Required for Decoupling with Integrated Capacitors -The much lower inductance of integrated decoupling capacitors enables less total capacitance to be used, since surface mount decoupling strategies typically string excess capacitance in parallel in order to lower the overall inductance. How much less, and how the total decoupling capacitance (integrated near the chip and as SM further away), should be optimally arranged is not known.
- Achieve a Manufacturable 0.3 µF/cm^2 for Organic Substrates -
  This density might be accomplished by lowering the processing temperatures for ferroelectric dielectrics, decreasing the thickness of paraelectric dielectrics, or embedding high-k materials after they are formed.
- Develop High Ω/Square Thin Film Resistor Materials -
  There are now good materials for low range (100 - 300 Ω/sq.) such as TaNx, CrSi, and NiCr. However, there is a need for 1000 - 10,000 Ω/sq. and no easily manufactured materials are available at this time.
- Solve the Problems with PTF Resistors -
  The mechanisms of value drift and reliability are well understood. Once they are solved, the low price and equipment requirements of PTF (polymer thick film) resistor material would make it very attractive for integration relative to thin film materials.
- Yield and Reliability of Large-Area Thin Film Embedded Caps -
  High-value integrated capacitors might have large areas of over 1 cm^2. These large aspect ratio films might be prone to mechanical damage from CTE (coefficient of thermal expansion) mismatch, bending, and ESD (electrostatic discharge). Improved reliability is often cited as a reason for integrating passives, but new failure mechanisms will certainly be present in the new technology.

Recommendations For Future Work

The following needs will be critical in the future:

- Embedded Passives
  - Establish HDI North American infrastructure (Microvia technology)
  - Conduct capacitor and resistor materials research
  - Develop design tools
  - Develop testing and trimming technology
  - Ensure technology sustainability to reduce probability of obsolescence
- Integrated Passive
  - Develop standards through EIA
  - Establish standard parts

Product Lifecycle Information Management

The following are areas that need improvement in the future:

- Develop IT enabled collaborative commerce among multiple trading partners -
  R& D is needed to raise IT system performance levels, harmonize data, and establish ways to exchange standardized decision support information. Not all suppliers have the infrastructure, tools, or on-site expertise to re-engineer, electronically enable, and manage all of the required supply chain activities. In order to develop a

trusting environment among competitors, methods to assist information exchange between EMS providers and the OEMs that manage critical component acquisition are needed to enable the EMS providers to plan their production and deliver as expected. Standard processes should be developed and adopted to manage shifts in production capacity and to extend visibility to all parties when manufacturing crosses regional and national boundaries.

- Improve the effectiveness of factory information systems -
  Methods to design, deploy, and operate FIS for a virtual factory must be developed. There is a need for the development, extension, and adoption of applicable industry standards concerning information exchanges, and trading partner interactions need to be developed. A definition of how virtual factories should be managed at the FIS level is needed. Getting the required information accurate and then distributing it to the right people in the supply chain at the right time in a usable format is a key goal.
- Establish guidelines for making sourcing decisions in the supply chain -
  Almost every OEM, and often every division or department in an OEM, has its own tools and approach to doing the analysis required to make data-backed sourcing decisions. The majority have been developed in house from trial and error. When companies get involved in outsourcing decisions, they often start with the simplistic approach of comparing costs of in house and outside. They make inherent assumptions and often ignore key attributes of supply chain performance that go beyond just price. Some of these attributes are:
  - The supplier's ability to deliver - there is often an implied assumption that you will get the same performance out of each alternative
  - Demand variability and the ability of the Supply Chain to respond
  - Information management systems integration capability - how quickly information connections can be set up for things such as direct routing of orders and confirmations
  - Freight modes, freight lane cycle time, costs, performance, and transportation costs
  - Local stability
  - Government policy
- Duties and tariffs, etc. -
  The typical evolution of the level of sophistication goes from comparing unit cost to comparing landed or delivered cost, and ultimately to a sophisticated model that allows for variability in numerous factors. Research is needed to identify the tools, best practices, and education that would enable practitioners to jump into sophisticated supply chain modeling without going through trial and error that leads to bad decisions. Education would also sensitize executives to the need for more complete supply chain analysis for the decisions and different metrics for the teams making these decisions.
- Environmental Issues -
  OEMs need to integrate environmental quality into their supply chain. They need to measure and benchmark their suppliers' environmental behavior in key areas such as implementation and continual improvement of an environmental management system (EMS), environmental performance with respect to efficient use of resources (materials, energy, water, wastes, emissions, etc.), and eliminating the risks of using hazardous substances. Suppliers who implement an effective EMS ensure that processes are in place to continually decrease the environmental life cycle impact of their products, operations and services. This enables improvements in areas such as natural resource efficiency, environmentally hazardous substance management and reduction, and full lifecycle management. Measuring and benchmarking suppliers in environmental performance enables decreased environmental impact and cost reductions through more efficient use of resources. Life cycle analysis (LCA), although very effective, can be quite data intensive and time consuming to undertake. Product take-back regulations will need to be addressed by OEMs in their product designs (e.g. design for disassembly) and in the total cost of ownership. Effective strategies will have to be implemented to meet the requirements of these take-back programs in different countries and with varied product mixes and materials contents. Materials content/declaration information derived from the supply chain will have a critical role in knowing the environmental history/traceability of products and their various components. Here, development of appropriate "industry standards" may have a key role.

Rf Components

Critical Issues Requiring Development:

- Medium power, low loss, high selectivity filters are a cost, weight, and size bottleneck to consumer and portable products, a problem to which there is no immediate solution.

- The advent of new wireless communication bands (IMT-2000, WLL (wireless local loop), (etc.) are likely to render the present radio architecture of using multiple Pas (power amplifiers) in one handset obsolete.
- Improvements in RF filter technology are not occurring rapidly enough to meet the cost/performance demands of both the portable and infrastructure product sectors.
- The rate of improvement in Analog-to-Digital Converter (ADC) technology is not fast enough to enable the implementation of digital linearizers in portable units.
- The rate of improvement in antenna design and development is not fast enough to meet the implementation needs of portable units like software defined radios and dual-band, dual-mode radios.
- The lack of integrated design and simulation tools (circuit, electromagnetic, thermal, mechanical, manufacturing, etc.) is slowing the trend toward higher functionality in mixed-mode wireless chips and modules.
- Second-source foundries for compound semiconductor IC manufacturing are lacking.

Test, Inspection, and Measurement

As with the last roadmap, several technologies exist that should be evaluated for use in other areas of test and inspection, including the following alternative strategies:

- Electromagnetic Signature -
  An extension of near-field scanning technology for diagnostics and signature analysis has been proposed as a means for non-contact testing over a spectrum of uses, including printed circuit boards. This extension requires the integration of a number of technologies and resolution of some practical considerations to ensure ongoing competitiveness against existing AOI/AXI technology and its adoption into the production test environment. The one significant benefit it may have, particularly in the area of RF, High Performance or Harsh Environment, is that it potentially could offer performance as well as structural test information. Important areas for research and development include probing compliant arrays with hybrid probes using both E-field and H-field to improve resolution and reduce analytical ambiguities. Smaller probe arrays may possibly be embedded in membranes for greater resolution. New probe technologies are needed to extend the range to GHz bands. Additionally, development of at-speed methods of functionally stimulating units under test, through advanced signal injection techniques (which may, in part, rely upon industry-wide consensus on DFT). Another need is the development of powerful image analysis software that enables an integrated system to detect, isolate, and evaluate faults rapidly. These innovations include de-blurring algorithms for improving resolution (by 3x-5x) through processing array signatures. Finally, we need to ensure that the probe arrays and software can be integrated into affordable platforms for testing a wide spectrum of electronics, ranging from chips with custom test fixtures, through single-chip and MCM (multi-chip module) packages, to bare and populated boards.
- Acoustic Microscopy -
  Acoustic microscopy was introduced in the late 1980s. In operation, focused high frequency acoustic waves are reflected from internal surfaces, interfaces or voids, typically in a pulse-echo mode where the attenuated and phase-shifted signals reflected from internal interfaces are interpreted using signal processing software. As an analysis tool at the device level, acoustic microscopy has demonstrated success in areas such as cracks and lid-seal flaws in ceramic flat-packs, separated gull-wing solder fillets, popcorn cracks in plastic packages, and voids in molding compounds. Die tilt and de-bonds from plastic to die and from plastic to lead frame are examples of defects effectively revealed via acoustic microscopy imaging (AMI) techniques. While it has equally been used for finding bad solder joints and imperfect BGA solder fillets or solder bumps on flip chips, it has not been applied as a board level test technology. Although visual inspection and electrical tests can detect most defects, and X-ray and thermal imaging can provide significant detail, certain defects and internal features consistently resist discovery by these methods, prompting the potential need for research in alternative technology.
- Photoelectric Effect -
  This technique uses a high powered UV laser to generate secondary emission of electrons that can be simulated and measured from a grid that is immediately above the board under test. This technique is targeted at bare boards and by applying charges to nodes and looking at stray charges and discharge rates, shorts and opens can be detected. These systems will be priced in the $500K to $1M price range.
- E Beam Test Systems -
  This technique is very similar to Photoelectric, with the bare board placed in a vacuum and steerable electron beams used to produce secondary electron flow. Grids can be on both sides of the board to act as source and detectors to find both shorts and opens. While lagging behind photoelectric, the technology is well known and can probe 2 mil pads and make more than 1000 tests per second.

- Thermal Imaging -
  In this case, a PWB is stimulated by elevating the temperature. Heat pattern flows of the boards, including solder connections, can be analyzed using infrared (IR) imaging. The time-temperature pattern is measured against a good joint and opens and shorts can be detected. Even marginal cases can be detected. The issue with this type of testing is test time, with 10 to 20 minutes required to heat and cool the unit under test.
- Plasma Based Testing -
  The plasma head for this technique needs to be mechanically staged similar to a flying probe system but the final probe is replaced by plasma generated by a high power laser. Ionized particles create an electrical pathway to the UUT where conventional stimulus and measurement can be performed. This is a non-contact testing technique that builds on flying probe technology having potentially finer resolution.

Thermal Management

Research Needs

The continued development of new and improved thermal management technology will require the combined efforts of industry based development and university based research with a focus on practical application. Extensive heat transfer, thermo-fluid, and thermomechanical research is needed to define new opportunities (i.e. path breaking) and to improve predictability and reliability (i.e. gap-filling). Research outcomes required to satisfy the thermal technology needs identified in the previous section are outlined below:

Thermal Spreaders

- Inexpensive, high thermal conductivity materials (possibly composites) offering a closer expansion match to the TCE of silicon
- Algorithms for optimizing thermal/thermomechanical design of thermal spreaders
- Techniques for achieving improved thermal spreading within a chip to alleviate hot spots due to localized high heat flux concentrations
- Correlations and analytical models of dry-out and rewetting of micro-channels and micro-porous structures to facilitate design of micro-heat pipes

Thermal Interfaces

- Thermal pastes, epoxies, and elastomers loaded with high thermal conductivity nanoparticles
- New interface materials based on carbon nano-tubes and other materials
- Novel techniques and materials to minimize interfacial stresses
- Correlations and analytic relations to predict fatigue life of bonded interfaces
- Standardized method to characterize thermal performance of interface materials
- Self-contained solid-to-solid phase change materials or micro-encapsulated materials as suitable interface materials for a range of applications including harsh environments

Heat Pipes

- Flexible heat pipes
- Heat pipes that handle high heat fluxes
- Low cost heat pipes that can transport heat effectively over large distances (>0.5 m)
- Designs to reduce the gravitational orientation impact on heat pipe efficiency, especially for avionics applications
- Heat pipe technology capable of withstanding harsh environments
- Sound numerical models and optimization tools for predicting the performance and operational limits, including dry-out, in heat pipes
- Correlations and algorithm for design of thermosyphons (i.e. wickless heat pipe)

Air Cooling

- Models and correlations to predict heat transfer in transition and low Reynolds number flow over packages and in heat sink passages
- Low Reynolds number turbulence models for use in CFD codes

- Heat sink design and optimization procedures for the minimization of heat sink thermal resistance, subject to mass and volume constraints
- Advanced manufacturing techniques for metal and composite material heat sinks
- Concepts for higher head-moderate flow, low noise, compact fans
- Novel, low power consumption, low acoustic emission micro-fans for forced convection cooling in notebook computers and handheld electronics, including low-frequency and ultrasonic piezoelectric fans
- Novel miniature fan concepts including low-frequency and ultrasonic piezoelectric fans for minimal noise emission and power consumption
- High pressure/high flow blowers with low acoustical power

Water Cooling

- Miniaturized components that have high reliability and provide enhanced performance (e.g. pumps and heat exchangers)
- MEMS and meso-scale components to create low-cost, low-noise, water-to-air heat exchangers
- MEMS and meso-scale components to create low cost, package-size cold plates
- Microchannel heat sinks with novel integrated micropumps to minimize package volume for high heat flux applications
- Methods to enable direct water cooling of chips or chip packages

Direct Liquid Immersion

- Single-phase and two-phase heat transfer correlations for new families of dielectric coolants
- Nanoparticles for addition to dielectric coolants to create a nanofluid with enhanced heat transfer characteristics
- Convective and phase change cooling correlations to account for highly non-uniform heat flux boundary conditions
- CHF (critical heat flux) models to account for highly non-uniform surface heat fluxes
- Characterization of boiling and two-phase flow in narrow passages and 3-D structures
- MEMS and mesoscale components to enhance convective, as well as pool and flow boiling, heat transfer
- Correlations and models for evaporative spray cooling heat transfer

Sub-Ambient and Refrigeration Cooling

- Highly reliable miniaturized components such as compressors, condensers
- and evaporators
- MEMS and mesoscale components to create low-cost, low noise refrigerators using solid-state, vapor compression, or absorption cycles
- MEMS and mesoscale components to create low-cost, package size cold plates using solid-state, vapor compression, or absorption cycles
- New thermoelectric materials and fabrication methods that can improve the performance of thermoelectric coolers

Low Temperature Refrigeration

- Application of Auto-refrigerating Cascade (ARC) systems to provide low temperature cooling for electronic packages
- Application of mechanically cascaded (2-stage) refrigeration systems to provide low temperature cooling for electronic packages

Recommendations

The following constitutes the major cooling technology areas for development and innovation:

- Low cost, higher thermal conductivity, packaging materials, such as adhesives, thermal pastes, and thermal spreaders need to be developed for use in products ranging from high performance computers to automotive applications.

- Advanced cooling technologies in the form of high performance heat pipe/vapor chamber cooling technology, thermoelectric cooling technology, direct liquid cooling technology, as well as high performance air-cooling and air-moving technologies, need to be investigated.
- Closed loop, liquid-cooling solutions which are compact, cost-effective, and reliable should be developed.
- High-performance cooling systems, which will minimize the impact to the environment within the customer's room and beyond, need to be developed.
- Advanced modeling tools which integrate the electrical, thermal, and mechanical aspects of package and product function, while providing enhanced usability and minimizing interface incompatibilities, need to be developed.
- Advanced experimental tools for flow, temperature and thermomechanical measurements for obtaining local and *in-situ* measurements in microcooling systems will be needed.
- It is further recommended that action should be taken to pool resources to fund cooling technology development, promote the involvement of university and other research labs and establish a closer working relationship with vendors.

Appendix B: Extract of Comments from the 2002 NEMI Roadmap Relevant to Nanotechnology

Design Technologies

- The size reduction of discrete devices has hit a wall at 0201 package size, with many facilities having difficulty maintaining optical recognition.
- The extension of Moore's Law beyond 2005 will require new packaging technologies to reduce the cost of packaging.
- Co-design of mechanical, thermal, and electrical performance of the entire chip, package, and associated heat removal structures is one of the key crosscut challenges.
- New materials, components, and processes need to be developed, qualified, and introduced in 2002-2006 to enhance recyclability, improve energy efficiency, and reduce ecological impact.

Manufacturing Technologies

- The component underfill process has provided faster flow times, but difficulties exist with reworkable and pre-applied underfill for standard SMT operations.
- For board assembly of optoelectronics to be competitive in North America, it is important to develop low temperature soldering and automated fiber handling and assembly.
- Board assembly will be challenged with providing material control and identification standards during the transition between lead free and eutectic materials and throughout the product life cycle.

Component/Subsystem Technologies

- There is a need for cost and performance models that help highlight the benefits of embedded passives.
- Faster improvements in RF filter technology are needed to meet the cost/performance demands of both the Portable and the Large Business Systems Product Sectors.
- Faster improvement in antenna design and development will help meet the implementation needs of portable units like software defined radios, dual-band, and dual-mode radios.
- Assembly processes and equipment are needed to support integrating electronics and optics into single packages.
- Technologies must be developed that support effective hybrid integration of components into lower cost, smaller, higher functioning subsystems.
- The development of improved optoelectronic subcomponents and materials that allow automation will be the key to expanding the market.

NEMI Technical Projects

- NEMI should create a nanotechnology presence to track the progress of its practical uses due to nanotechnology's potential for being highly disruptive to member companies.
- EMS companies need to take the lead in electronics manufacturing technology development, utilizing pre-competitive consortia like NEMI to leverage their R&D and technology deployment budgets. Continued cooperation with government and academia should also be adopted to help address the R&D gap.
- NEMI should establish new projects in 2002-6 to develop, qualify, and introduce new materials, components, and processes that will enhance recyclability, improve energy efficiency, and reduce ecological impact.

Materials Development

- A project needs to be developed in the interconnect arena to improve the dimensional stability of organic materials used in PWB manufacturing.
- A combination of materials and fabrication research is needed to support the development of monolithically integrated optics and electronics that take advantage of the electronics infrastructure.

- Technology development is needed in areas such as optical solders and board level wave-guides to enable more complex and higher density board level products.

Technology Development

- Fuel cell systems, lithium-metal/SPE technology, and thin-film batteries have the potential of providing very high energy density and specific energy. These technologies are recommended for further development on an R&D level. Fuel cell systems that operate near ambient temperature are a possible power source for portable electronic devices. Identifying the appropriate technology to store fuel for portable applications needs to be addressed, as does hybrid power system design.
- Disruptive technology (such as fuel cells) for overcoming substantive technical hurdles (e.g., developing batteries for electric/hybrid vehicles) offers a window of opportunity. In order to ensure success, North American manufacturers must be willing to invest with a long-term perspective in mind.

Appendix C: NEMI Overview

NEMI History

NEMI grew out of two separate efforts to recapture American leadership in electronics manufacturing. In 1993, the American Electronics Association (AEA) conducted a study (led by Mauro Walker, Senior Vice President and Director of Manufacturing at Motorola) on the U.S. Electronics manufacturing infrastructure. Based on the results of this study, AEA recommended that the Administration create a national initiative in electronics manufacturing, focusing on strategic electronic components and electronics manufacturing systems. The second effort originated with the National Science and Technology Council's Electronics Subcommittee (ESC), chaired by Lance Glasser, Director of the Electronics Technology Office at the Defense Advanced Research Projects Agency (DARPA).

In 1994, Dr. Walker and Dr. Glasser teamed up to initiate the creation of NEMI. Over a 10-month period, they met with representatives of government, executives from many of the industry's largest manufacturers of electronic home and business products, and executives from the suppliers that manufacture the constituent materials, components, and subassemblies. The first NEMI Roadmap was produced in 1994 and NEMI was incorporated in January, 1996.

NEMI Mission

NEMI is a North American based consortium dedicated to providing leadership for the global electronics manufacturing supply chain for the benefit of both member companies and the industry as a whole.

NEMI Organization

The NEMI Board of Directors (see fig.#1) defines the policy, strategy and direction of NEMI; has operational responsibility for the NEMI organization; is responsible for the NEMI Executive Secretariat; and reviews the performance of all projects and programs.

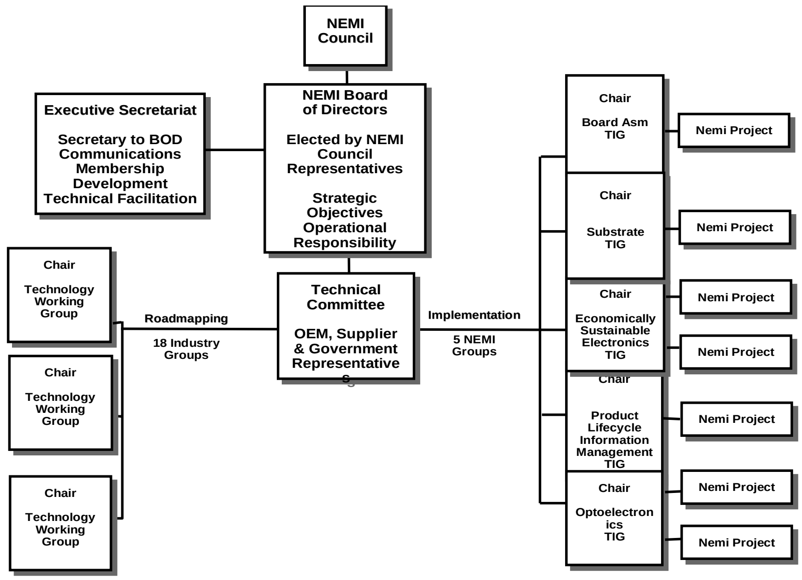
The Executive Secretariat includes the Executive Director/CEO and a small support staff. This group provides the administrative support for the organization, including coordination of meetings, maintenance of data bases, publishing and distribution of documents, providing assistance to the Technical Committee, and performing other necessary administrative duties.

The NEMI Technical Committee facilitates and coordinates all NEMI technical activities and is comprised of OEM and supplier representatives as well as government, university, and industry association representatives. The Technical Committee reports to the Board of Directors and Co-chairs of the committee are ex-officio members of the Board. The Technical Committee develops and maintains the prioritized NEMI Technical Plan; approves development and deployment projects; appoints Technology Integration Group and Project chairs; organizes, manages, and publishes the biannual NEMI Roadmap; and recommends priorities for potential university research programs.

The Technology Working Groups (TWGs), who report to the Director of Roadmapping, are responsible for developing the technology roadmap, identifying the technology gaps, and recommending key technical areas for the TIGs to work on. TWG membership is open to the entire industry, worldwide. Currently some 18 industry groups, along with 5 Product Sector Champions assist the Director of Roadmapping in roadmapping activities.

The Technical Integration Groups (TIGs), currently five in number, report to the Director of Planning and are responsible for developing the Technical Plan, identifying technology needs, and establishing projects to address them. TIG membership is limited to NEMI members.

NEMI Organization Chart



NEMI Organization

NEMI Deliverables

NEMI activities produce five key resources and benefits for North American electronics manufacturers:

- Roadmaps showing a projection of the needs of the electronics industry
- A list of identified gaps in the manufacturing infrastructure
- NEMI stimulates R&D projects to fill these gaps
- Integration projects designed to eliminate these gaps
- Encouragement of standards activities to speed the introduction of new technology

Standards

In the course of the project activities, NEMI work often affects existing standards or requires new standards to be written. Each project considers standards activities required before it is formally approved by the Technical Committee. However, NEMI does not choose to release or maintain standards. Instead, NEMI has developed relationships with existing standards organizations, such as IPC, EIA and IEEE , to develop, release and/or influence standards of interest to NEMI members.

Further Information

For availability of referenced documents (such as the latest NEMI roadmap or Annual Report) and other information on NEMI, please contact us at:

Voice - 703-834-0330

Email – info@nemi.org

Web site – www.nemi.org

Appendix D: Glossary

3D – Three Dimensional
ADC – Analog to Digital Converter
AESF - American Electroplaters and Surface Finishers Society, Inc.
AMI – Acoustic Microscopy Imaging
AOI – Automated Optical Inspection
ARC – Auto – refrigerating Cascade
Atm – Atmosphere
ATP – Advanced Technology Program
AXI – Automated X-Ray Inspection
B2B – Business to Business
BGA – Ball Grid Array
CAD – Computer Aided Design
CAMX – IPC Computer Aided Manufacturing Standard
CAPEX – Capital Expenditures
Cd – Cadmium
CD – Compact Disk
CHF – Critical Heat Flux

cm^2 - centimeter squared
CMOS – Complementary Metal Oxide Semiconductor
CrSi – Chromium Silicate
CrVI – Chromium
CSP – Chip Scale Package
CTE – Coefficient of Thermal Expansion
Cu – Copper
DfA – Design for Assembly
DfE – Design for the Environment
DfM – Design for Manufacturing
DfT – Design for Test
DIMM – Dual In-Line Memory Module
DNA - Deoxyribonucleic Acid
DPMO – Defects Per Million Opportunities
E Field - Electric fields, created by voltage and measured in volts per meter
ECE – Environmentally Conscious Electronics
EDA – Electronic Design Automation
EDI – Electronic Data Interchange
EIA – Electronics Industries Association
EICTA – European Information & Communication Technology Industry Association
EK – Electro – Kinetic
EMI – Electro Magnetic Interference
EMS – Electronics Manufacturing Services
ENIG – Electroless Nickel Immersion Gold Plating
EPA – Environmental Protection Agency
ESD – Electrostatic Discharge
FBGA – Flip Ball Grid Array
GaAs – Gallium Arsenide
Gb – Giga bit
GHz – Giga Hertz
H Field - Magnetic fields, induced by alternating current (AC) and measured in gauss or Tesla
HAMR – Heat - Assisted Magnetic Recording
HDI – High Density Interconnect
Hg – Mercury
High k – High Dielectric Material Used in Capacitors For Higher Value Capacitors
High n/sq – High ohm per Square

I/O – Input / Output
IC – Integrated Circuit
INSIC – International Storage Industry Consortium
IPC – Institute for Interconnecting and Packaging Electronic Circuits
IT – Information Technology
ITRS – International Technology Roadmap for Semiconductors
JIETA – Japan Electronics & Information Technologies Industries Association
KW/cm² - Kilo Watts per Square Centimeter
LCA – Life-Cycle Analysis
LGA – Land Grid Array
Low k – Low Dielectric Constant Materials Used with Copper Interconnects for Lower Delays in Integrated Circuits
LTCC – Low Temperature Co-Fired Ceramic
MEMS – Micro – Electro – Mechanical Systems
mm – Millimeter
MRAM – Magnetic Random Access Memory
MTBA – Mean Time Between Failures
N² - Nitrogen Gas
NEMI - National Electronics Manufacturing Initiative
NiCr – Nickel Chromium
NIST – National Institute of Standards and Technology
NNI – National Nano-technology Initiative
NPI – New Product Introduction
OE – Optoelectronics
OEM – Original Equipment Manufacturer
OPEX – Optoelectronics Expenditures
Pb – Lead
PBB - Polybromated Biphenyl
PC – Personal Computer
PDA – Personal Digital Assistant
PLIM – Product Life - Cycle Information Management
PTF – Polymer Thick Film
PWB - Printed Wiring Board
R & D – Research and Development
RF – Radio Frequency
SECs/GEM - Semiconductor Equipment Communications Standard (SECS) and Generic Equipment Model (GEM) standard
Si – Silicon
SIA – Semiconductor Industry Association
SiGe – Silicon Germanium
SIP – System in Package
SMT – Surface Mount Technology
SOA – Semiconductor Optical Amplifier
SoC – System on Chip
SPE – Solid Phase Epitaxy
SPM – Standard Process Modules
TaNx – Tantalum Nitrate
Tg – Glass Transition Temperature
TIG – Technical Implementation Group
TIM – Test, Inspection and Measurement
TIM – Thermal Interface Materials
TMR – Tunnel Magnetic Resistance
TWG – Technical Working Group
UBM – Under Bump Metallurgy
UF – Micro-Farad
UL – Underwriters Laboratory
um – Micron

UUT – Unit Under Test
VCSEL – Vertical Cavity Surface - Emitting Laser
W/cm^2 - Watts per square centimeter
WLP – Wafer Level Packaging
XML – Extensible Markup Language

Appendix E: Contributors

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