

High-Throughput RFIC Wafer Testing

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Abstract This paper surveys the state of RFIC wafer testing as performed on production floors today, and the trends and expectations for the future. Currently, most RF chips sold as known-good die (KGD) and relatively complex RFICs are tested at-speed at the wafer level. RF wafer testing is used to reduce the cost of scrap at the next level of packaging, and various test strategies are pursued to reduce test costs. The hardware options and tradeoffs for production testing are surveyed. Finally, the outlook for test cost, ATE resources, chip connection density, and for emerging technologies such as built-in self-test, are discussed.

I. INTRODUCTION

As the speed of wired and wireless communications systems increase, ICs and their packages will be pushed to run at higher frequencies and the highest possible data rates. At the same time, communications at microwave frequencies are becoming the norm for consumer electronic products. These forces are creating rapidly increasing demand for high volumes of low-cost microwave chips for consumer information appliances [1] and for highly integrated chips for communications system infrastructure [2]-[3]. Typical RFICs in this class today include RF functions for cell phone handsets, Bluetooth transceivers, chipsets for optical transceivers for 2.5 and 10 Gb/s telecomm and datacomm systems, and front ends for various wireless subscriber-loop systems. Last year TI estimated that 865 million cell phone handsets will be sold in 2003, and various market surveys expect over 500 million Bluetooth chips to be sold annually by 2005.

RF test systems capable of high throughput--loosely defined here as capable of functionally testing a typical RFIC on the order of one second--became commercially available in the mid 1990's. The first microwave chips tested at high volumes were relatively simple, including switches, amplifiers, mixers, LNA/mixer combinations, etc., and almost all of these were RF tested only after being packaged in small SOIC packages. Since 1999 there has been a steady increase in the number high-volume RFICs that are tested on-wafer instead of, or in addition to, being tested at the package level.

II. RF WAFER TEST ECONOMICS

A. Engineering vs. Production

Microwave measurements for process, device, or module engineering are typically driven by the need for process characterization and development, accurate CAD models of circuit elements, or prototype debugging. By contrast, production IC test is driven by the need to screen ICs for an acceptable quality level at the lowest total cost. Since the lowest die cost is achieved by trading off die shrinks versus yield, there will always be a need to sort out the defective dice. ICs may be tested before or after packaging, or both.

B. Known-Good Die

When a bare die is sold for assembly into a multi-chip module, it is typically far cheaper to assure the die quality before assembly, so that the module needn't be reworked. Such die require final testing as die or in wafer form; in the case of RFICs, the wafer form is sufficient and is far easier to handle than dice. A die thus tested is often referred to as a known-good-die, or KGD. Depending upon the application, test can increase the value of a bare die by 50% to 2000%. Note that some wafer-level packaging or chip-scale packaging approaches similarly do final test in the wafer form, and then saw up the wafer. [4]

C. Simple Packaged RFICs

Small RF chips are commonly packaged in an SOIC-style package with 8 to 20 leads. These packages cost about \$0.01 per lead, so this packaging cost times the yield loss is the main cost that can be saved by doing wafer testing. The yields on small chips can be very high, so almost all such chips are RF tested only after packaging. Some high-yield parts are not even screened by dc testing before packaging.

D. Complex Packaged RFICs

More highly integrated RFICs, such as receiver or transceiver functions, naturally have lower yields and also require more expensive packages (more pins) than single-function RFICs. At some point the yield loss times the packaging cost exceeds the costs of adding a wafer-level test step. The burdened cost of a production test cell is typically on the order of \$200 per hour, so a 100% utilized test cell costs around 5 cents per second; additionally, a medium-complexity RF probe card will cost on the order of 1 cent per contact cycle. Additional decision factors include the savings of getting immediate feedback about yields, reducing the risk of bad lots in a two-week packaging pipeline, reducing the test time at final (packaged) test, and the practical issue of having sufficient RF wafer test expertise on the test floor.

E. Test Strategies

Test cost reduction strategies generally fall into three categories: test less, test earlier, or test faster. The “test less” approach cuts out test steps that are duplicated at other steps (such as wafer vs. package test), or are unnecessary as determined by correlation data. As a design or process matures in production, the number of tests performed is often empirically reduced, without losing test coverage. Higher integration levels automatically test less, to the extent that a string of circuit functions can be tested end-to-end instead of each individually (the internal nodes become less accessible anyway). “Test earlier” strategies reduce costs of adding value to an already defective part; examples include more performance predictions from PCM measurements, or RF performance screen at the wafer level, followed by only continuity testing after packaging. The “test faster” strategy increases equipment throughput by increasing up time, by decreasing test times (similar to test less), or by testing two or more devices in parallel, thus improving efficiencies of capital and operator time. DRAM’s are routinely tested 16 or 32 at a time, and some RFICs are tested two or four in parallel now.

In most production IC test environments the repeatability of measurements is valued over the absolute accuracy--for example, a common setup verification test is to probe a reference wafer to see if the yield is what was measured in the past. Since the whole objective is to screen parts at the lowest cost, there are often many basic problems on the test floor that go unsolved in the name of urgency or saving money, even though a fix would save more money.

III. RFIC PRODUCTION WAFER TEST TODAY

A. ATE

Many RFIC test systems are built up from “rack-and-stack” bench-top instruments, but the data transfer rates limit their throughput and cost efficiencies of such systems are not as good for high volumes as dedicated ATE. Almost all IC ATE vendors offer some RF test options today [5]. The number of RF ports varies from two, for a minimal system for power amplifiers, to 20 or more for complex RFICs. The types of basic RF stimulus and measurement capabilities include S-parameters, noise figure, power, and spectrum analysis. More complex measurements, such as spectral regrowth or mixer distortion, are typically standard functionality in the software. All ATE systems provide dc power supplies for powering and controlling the DUTs and measuring various voltages and currents, some pulsed. As RF front-end chips start to integrate IF functions, RF subsystems are being added to mixed-signal ATE systems, which typically provide analog signal stimuli such as arbitrary waveform generators (AWGs) and voltage measurements using high-speed digitizers.

The test cell is completed by a device handler, which for on-wafer measurements is an automated prober, an interface, and a probe card, which together connect the ATE test head to the die on the wafer. There is usually little in the autoprobe that is different to support RF measurements versus lower frequency measurements. Fig. 1 illustrates an ATE system and an autoprobe.



Fig. 1. An Agilent 84000 RFIC test system and Electroglas 4090 autoprobe. The test head is raised from its position of operation. Not illustrated is the operator’s workstation.

B. Interfaces

The interface must connect the ATE test head to the probe card. There are three general types of interfaces used with RF ATE [6]: a cabled interface, a tower fixture, or direct docking. Cable interfaces simply connect the test equipment to the probe card through a bundle of RF and dc cables; this is typical of rack-and-stack systems. While this is the cheapest to configure, disadvantages include the RF loss, complexity in reconfiguring the setup for another part, and intermittent contacts in the cables or connectors. A tower fixture, as in Fig. 2, is replicated for each probe card and spare. This provides mechanical isolation between the test head and the probe card through coax cables. It is the most expensive type, but provides a rugged fixture that can be quickly changed for different ICs. Direct docking, wherein the probe card directly plugs into the test head, minimizes cable losses but does not provide mechanical isolation and can limit the space available for components on the probe card.

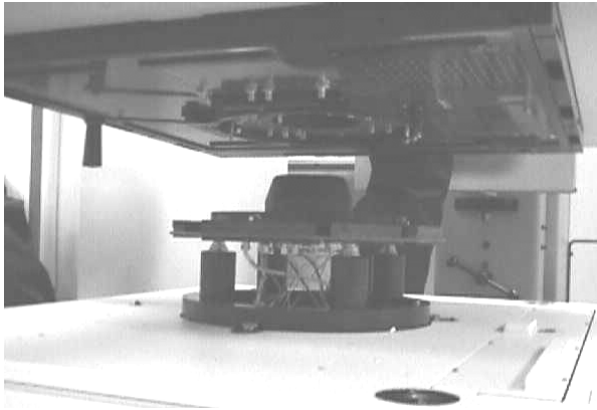


Fig. 2. A tower fixture mounted to the autoprober, with the ATE test head above it. The blind-mate RF connectors and the hole in the center of the head for microscope access are visible.

C. RF Probe Cards

An RF probe card for complex ICs must provide many wideband signal lines with low reflections, very low and repeatable common-lead inductance, low power supply impedances, versatile probe tip patterns, and customized circuitry very close to the chip under test as well as on the probe card [6]. At this point, it appears that a lithographically printed membrane-style probe is required to practically achieve these features for more than just a few probe tips at microwave frequencies. Fig.

3 illustrates a membrane probe customized for an unmatched L-band power amplifier chip [7]. In addition to RF performance, a production probe card must be rugged and provide highly repeatable RF connections from one die to the next and one probe card to the next. When contacting ICs with aluminum bond pads (as most silicon ICs use), the probe tips must also reliably scrape through about 60 angstroms of oxide on the aluminum pads to make a low contact resistance to the aluminum [8]. Probe card lifetime expectations are on the order of 1 million contact cycles; this is much easier on gold pads than on aluminum



Fig. 3. An RF membrane probe core. This interfaces the chip under test to the probe card board. Probe tips around the rectangle in the center connect to a 50-ohm input line (lower right), a bypass capacitor (lower left), and a 2.5-ohm matching network and bias chokes (top).

To decrease test costs, parallel RF testing is emerging at the wafer level. Fig. 4 shows how a membrane probe contacts four simple RF die in a row.

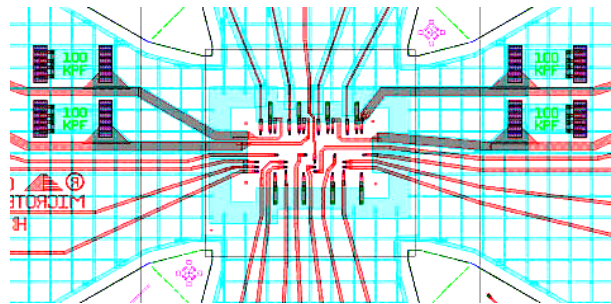


Fig. 4. Layout of a membrane probe core for X4 testing.

D. RF Calibrations

The vast majority of high-volume RFICs operate at frequencies below 3 GHz. For these frequencies, most RF ATE systems use a two-tiered calibration approach, where the first tier is the test head out to its coax connectors. The second tier is the networks of the fixturing from the coax ports to the probe tips. The first tier is typically calibrated periodically (as infrequently as every six months for some ovenized test heads) as a multi-port VNA (in port pairs) with coaxial standards. For three-port devices, multiple two-port calibrations are typically used, since the port termination impedances interact very little in typical devices (e.g., switches).

The second tier of the calibration is often as simple as a scalar loss correction for each port, if no phase data or vector corrections are required. Vector measurements of the second tier (assuming just transmission lines to the probe tips) need only measure one-port standards at the probe tips, since the thru calibrations occurred at the first tier. Note that the second-tier calibration is a complete characterization of the signal lines, useable for fixture quality assurance.

Many RFICs utilize differential signal connections at the signal ports; to interface to the single-ended ATE ports, baluns can be connected on the probe card circuit board. In this case, the even-mode power is usually assumed to be negligible and differential calibration elements (such as a 100-ohm load resistor between the probe tips) can be used to calibrate the second tier at the probe tips.

IV. RFIC TEST ROADMAP

Table 1 is an RFIC test roadmap from the 2000 NEMI Technology Roadmap [9]. An inescapable force in ICs is the need for continuous cost reductions, especially for low-cost products. ATE per-channel costs will continue to decrease for a given functionality, but the functionality per channel continues to rise. More complex chips will allow testing of more functions in cascade, but more parallel test is implied for such dramatic cost reductions.

As systems on a chip (SoC) technology matures, a large digital chip may integrate a microprocessor, a large DRAM, various data interfaces, and an RF transceiver such as for Bluetooth. This trend is one force driving general-purpose ATE systems, typically referred to as "SOC test". As listed in the table, digital logic and RAM test functions will be the norm, and high power dissipation will be required for some SoCs. The digital testing will require at least 100 digital IO's for DFT chains (see below). General-purpose testers also have advantages for allowing better ATE utilization with a shifting product mix, standardizing fixturing, and minimizing training. The obvious disadvantage is cost, but some ATE vendors are offering to charge only when the various tester resources are being used.

The third parameter in the table is the pitch of microwave BGA packages, which will be tightest at high frequencies and for the highest density requirements. More compliant microwave probes will be required for measurements on such packages.

Parameter	2001	2003	2005	2011
<i>Test cost (for a given function, relative to 2000)</i>				
Low-cost	0.5	0.25	0.12	0.02
Handheld	0.7	0.35	0.18	0.03
Cost-performance	0.9	0.8	0.7	0.5
Harsh environment	0.7	0.35	0.18	0.03
<i>ATE resources required</i>				
Low-cost	RF/analog/digital	Add RAM, X4	Add 50W, X8	Add X32
Handheld	RF/analog/digital	Add RAM, X4	Add X8	Add X32
Harsh environment	80 GHz RF	X2	X4	X16
<i>BGA socket pitch (mm)</i>				
Low-cost (3 GHz, 0.5 nH)	0.7	0.5	0.4	0.3
Handheld (3 GHz, 0.5 nH)	0.5	0.4	0.25	0.2
Harsh environment (77 GHz, ~0.05 nH)	0.2	0.2	0.2	0.2

Table 1. Production RFIC Test Requirements Solutions being pursued No known solutions

Today the testing and debugging of a large logic IC (>200,000 gates) almost requires design-for-testability (DFT) functions built into the logic [e.g., 10]. This usually takes the form of long chains of additional shift registers that can subdivide the overall chip into many small pieces and test each gate and register in each piece. The additional chip area used by the DFT gates is typically ~3% of the total area.

DFT is rarely used for analog signals, though internal analog nodes are often multiplexed out to pads for stimulus or measurements by putting the chip into a test mode. RF nodes are more difficult to access, but this can be used in some cases.

Built-in self-test (BIST) is today being used in its simplest forms to test blocks of embedded DRAM in logic chips. As larger DRAM blocks are used, the ratio of area used by the BIST gates will continue to decrease. Some applications, such as low-volume ASICs, will adopt BIST for testing logic functions in IP blocks. Analog BIST is being developed, but RF BIST is rarely even considered. However, it may become practical in low-performance radio systems to loop a chip's RF transmitter to its receiver with some extra circuitry for a level of self-test functionality.

V. SUMMARY AND OVERALL TRENDS

- ASIC complexity is doubling about every four years, and CMOS device cutoff frequencies are doubling about every five years.
- Test at wafer probe versus final test saves package scrap and provides quicker yield feedback to the fab.
- RFIC on-wafer test is growing, driven by known-good die requirements and more efficient screening of highly integrated die.
- Multiple vendors provide RF ATE systems, package handlers, contactors, probers, and probe cards.
- RF test functions are being added to mixed-signal test systems and will evolve into just one of the functions of a general-purpose SOC tester.
- RFIC test will become increasingly parallel, especially for low-cost devices.
- Some elements of DFT and BIST methodologies may be applicable to RF test in the foreseeable future.

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