

# The Impact of DENSITY and FREQUENCY on Organic Interconnect Substrates

In the just-published edition, the Nemi Roadmap calls for increased wiring density and better high frequency characteristics. Will it spell trauma for fabricators? by JACK FISHER

Organic printed boards continue to be the workhorse for pin-in-hole (PIH) and surface-mount technology, accounting for more than 90% of the interconnects used today. The nature of boards is likely to change significantly in the next few years, however, as performance demands of electronic systems increase, and the density and complexity of the entire interconnecting structure swell with them.

Besides electrical functionality, the interconnecting substrate must provide circuit signal matching, thermal management, and mechanical support. These characteristics are no longer trivial. Furthermore, the role of interconnect continues to grow, performing circuit functions beyond simply pro-

viding interconnection wiring.

In its recently published 2002 roadmap, the National Electronics Manufacturing Initiative identifies several trends that will affect board requirements in the next several years. The key factors continue to be increasing density and higher frequencies, which have far-reaching effects that pose challenges for board fabricators. Printed boards of the future must offer, among other things, increased wiring density (more layers with improved build-up microvia technology) and better high frequency characteristics – both better materials and improved impedance control. Another development that can be expected to have a significant impact on board fabrication is the drive toward lead-free solders and bromine-free laminates.

The growth of array packaging has exceeded predictions of the 2000 NEMI roadmap and is driving increased wiring density, which demands the use of very small vias on tight grids, as well as fine line wiring with equivalent spacings and on multiple levels. The ability to produce small vias and fine conductors is increasing as manufacturers upgrade the drilling, plating, and etching equipment; however, on a global scale, the volume is still small.

Table 1 shows the projected interconnection needs of the various product sectors. (These sectors are used by all the key electronics industry roadmaps.) There has been a dramatic increase in maximum component density (in parts per cm<sup>2</sup>), and maximum I/O density (in I/Os per cm<sup>2</sup>) in the past four years. The numbers in the table reflect the increase between 2000 and 2002.

Tomorrow's interconnecting and mounting structures will require greater precision when it comes to conductor placement and definition and in the dielectric properties of the material. Moreover, the substrate will likely require that

**TABLE 1.** Maximum Component Density Requirements, 2000 and 2002

PRODUCT TYPE	MAXIMUM PARTS PER cm <sup>2</sup>		MAXIMUM I/O PER cm <sup>2</sup>	
	2000	2002	2000	2002
Year of Roadmap Publication				
Consumer (low cost)	23	26	160	208
Handheld	39	50	175	280
Office Systems Products (cost performance)	30	45	160	220
Large Business Systems (high performance)	10	17	156	237
Automotive (4-layer with microvia)	50	60	40	50
Military (10-layer with blind or buried vias)	45	70	100	150
Super Component (8-layer with microvia)	31	42	204	250

the interconnecting structure already contain the materials necessary to attach components (e.g., solder bumps, palladium-coated lands, conductive adhesive).

Table 2 represents the status of technology today. As indicated, 60 µm conductor (line) width and spaces on conventional FR-4 processes are available in limited production quantities, while 40 µm lines and spaces are available only from very select fabricators. Microvia technology is used in most of the component board or multichip or few-chip module substrates; however, they are not used in conventional printed boards, mainly because the cost of microvia has not yet come down to the cost of standard technology but also because products for those markets permit more liberal tolerances. This fact is changing as designers find that layer count can be reduced by adding HDI layers. Today, microvias show up in threshold and state-of-the art products, as demonstrated by their use in high-end laptop computers and video recorders, and in special niche markets. These products are being produced with >75 µm lines and spaces. Table 3 shows current capabilities for component boards.

To increase performance of electronics while reining in costs, component density must be increased. Thus, the total number of components attached to a single assembly is growing, while the available mounting real estate is shrinking. In addition, the number of functions per device is increasing. With increased complexity comes increased I/O count and reduced contact pitch. Reduced contact pitch represents challenges both for assemblers and bare board manufacturers. Assemblers have handling problems, not to mention difficulties with coplanarity and alignment. Fabricators encounter land size issues, solder-mask difficulties, and electrical test problems.

Although use of high I/O components on an assembly represents a fraction of the total number of components in place, it is a big factor within the industry infrastructure. With the advent of multi-device subassembly (MDS) components in an array format, the pitch and I/O will also be a challenge to the board fabrication function (both the product board and the MDS board). These high I/O components set the process for bare board manufacturing in imaging and etching, testing, surface finishes, and so on. They determine the materials used for fabrication and also drive assembly process improvements in a similar manner. Use of high I/O components is ramping at a very high average rate, between 30% and 70% per year.

Assembly has advanced to a stage where most compo-

nents are available only in surface mount form. The increased device complexity has been a primary driving factor for SMT. In order to keep the component package size down, component lead spacing has decreased (e.g., to 0.65 mm from 1.27 mm). Further increases in semiconductor integration (VLSI) – more than 196 I/Os – can drive packages to even narrower perimeter lead spacing such as 0.5, 0.4, 0.3, and 0.25 mm. The array package format has become the favorite for high I/O count devices. These package styles have a pitch that is more forgiving in the assembly processes.

Ball and column grid arrays are now being standardized on 1.5, 1.25, and 1.0 mm pitch. CSP array packages are standardized starting at a pitch of 1.0 mm and dropping to 0.8, 0.75, 0.65, and 0.5 mm matrices, with proposals to go to 0.4, 0.3, and 0.25 mm. The via pattern for the board requires tighter feature control as the pitch for BGA, mini-BGA, and CSP becomes smaller. There is a question as to how many lead pitches are required between 1.0 and 0.5 mm. One other concern is that the ball diameter is changing with each change in pitch. The semiconductor packaging industry has been solving its problems with little apparent concern for substrate manufacturers and contract assemblers. This may be changing as discussions have started to influence a preferred pitch and routing conditions.

As the complexity of ICs forces the adoption of surface mounting, the board will also be affected. With more of the circuit customization going into silicon and with the component package size increasing, the printed board size may also change. However, the higher I/O demand will require multi-layer or HDI (microvia) designs to support the wiring needs for closely spaced devices, or to provide the escape routing from internal connections of array component patterns. Both sides of the board may be needed to place all the components. There will also be an increased demand on the board to serve the need for power dissipation.

As the pitch changes, it becomes more difficult to produce the board, and high-density boards become mandatory. Requirements for high-pin-count single device module component boards, in which the board provides interconnections from the die to an array pattern or a multichip module, are the most complex situations. Miniaturization of the interconnecting products produces value by providing more interconnect density in the same size package or more interconnect density in a smaller package.

In addition, industry data indicates that cost improve-

**TABLE 2.** Current State of Substrate Technology for Product Boards

	CONVENTIONAL <sup>1</sup>		LEADING-EDGE <sup>2</sup>		STATE OF ART <sup>3</sup>	
	FR-4	MICROVIA	FR-4	MICROVIA	FR-4	MICROVIA
Line width/line space	100 µm/100 µm	n/a	60 µm/60 µm	50 µm/75 µm	40 µm/40 µm	35 µm/35 µm
PTH hole size (unplated)	300 µm	n/a	225 µm	75 µm	150 µm	40 µm
Drill capture land size	450 µm	n/a	325 µm	175 µm	300 µm	90 µm
Buried passive components	No	No	Very limited	Yes	Yes	Yes

1. Available from 85% of fabricators.  
 2. Limited production; available from 15% of fabricators.  
 3. Available from less than 1% of fabricators.

ments in high-density multilayer boards are made every year at an average rate (CAADR) of approximately 7% per year. The U.S. board industry experienced a steep drop in orders during 2001 and still suffers at times from differences in currency rates and business problems in Asia.

Microvia board cost is currently set by density. Today, the total cost for a high-density board with microvias is, in some cases, approaching the same as the total cost for an FR-4 equivalent density board. However, there is still a much broader range of prices in microvia technology than there is for regular FR-4 technology. High-density board costs, both for printed and microcircuit boards, will decrease as more technologies mature and additional fabricators begin to manufacture these technologies.

### Frequency Drivers

As the processing speeds of computers and modules reach 400 MHz, signal speed and integrity become paramount. The high speed is mainly for the microprocessor. The interconnecting buss speed requirements are somewhat less, in the neighborhood of 100 MHz. The need for greater capability will be apparent as systems designed to run above 200 MHz are built on FR-4. But the design becomes more difficult as frequency increases. As processing speeds continue to increase, pressure will continue to lower the dielectric constant (Dk) and also lower the dissipation factor (Df) of the material.

Advanced materials technology is needed to provide robust solutions from a variety of polymer and carrier systems, which often use thermosetting polymers. For example, cyanate ester provides signal transmission speeds of 114 cm/ns compared to 100 cm/ns in typical FR-4 epoxy material. Lower Dk and Df provide several solutions when selecting advanced material technologies. Lower Dk enables faster conductor signal speed and thinner interconnects for the same conductor geometries. Lower Df means improved signal integrity and less signal loss with higher frequencies. Some newer materials require characteristics that deal with not only their electrical properties but also mechanical ones. Since most Nemi emulator products are cost driven, their properties consider FR-4 as the basic foundation. New formulations of epoxy resins are measured as to their price parity with FR-4.

Embedding passive devices like resistors and capacitors is another hot topic. This market is just starting to develop and there are several different directions that the technology could migrate. At least one major OEM is counting heavily on buried passive technology in its future, and several others have ongoing developmental programs in the works. For the PCB, embedding resistors and capacitors is not revolutionary, but it is difficult and it will take a few years before we realize its full impact.

### The Heat is Rising

There are two significant things happening today in the organic substrate materials industry. One is the drive to use lead-free solder and the other is the drive to use bromine-free laminates. Although both activities are controversial, we will assume for this discussion that the migrations to lead-free and bromine-free will occur.

**TABLE 3.** Current State of Substrate Technology for Component and MCM Boards

	CONVENTIONAL <sup>1</sup>	LEADING-EDGE <sup>2</sup>	STATE OF ART <sup>3</sup>
Materials	FR-4	High Temp FR-4	BT Epoxy
Line width/ line space	75 µm/75 µm	60 µm/60 µm	50 µm/50 µm
PTH hole size (unplated)	200µm	150 µm	100 µm
Drill capture land size	400 µm	300 µm	300 µm
Buried passive components	N/A	No	Yes

1. Available from 85% of fabricators.

2. Limited production; available from 15% of fabricators.

3. Available from less than 1% of fabricators.

The constraint of the higher melting point for no-lead solders is not as significant to the board as is the requirement for bromine-free laminate. For the board to withstand higher solder temperatures, it is necessary to increase the laminate's thermal characteristics. Laminates with higher thermal capabilities are already readily available. Higher Tg and superior time-to-delamination laminates have been qualified by Underwriters Lab. However, these laminates may carry a slightly higher cost. The test, then, is to identify the minimum thermal characteristics that will withstand the higher temperatures in an attempt to minimize the cost impact.

Bromine-free laminates will necessitate extensive testing. Testing must be done for reliability, processability, and UL certification. This process is very costly and lengthy. Laminates that are bromine-free are now becoming commercially available. These laminates first showed up in Japan. Testing is ongoing. The most expensive laminates, such as polyimide, provide the highest performance but are very costly. The least expensive laminate is FR-4, but it does not have all the qualities of the high-performance laminates. Today, bromine-free laminate is not the lowest-cost laminate, but more use may help to reduce cost.

We continue to see a much broader range of prices in microvia technology than there is for regular FR-4 technology. And there is a genuine trend toward lead-free solders and bromine-free laminates but there doesn't seem to be a drop-dead date. It will be a long, slow integration.

Today's fabricator can expect to see a continued push by OEMs to get higher density, high-layer-count PCBs. There will be an effort to include high-performance materials in the high-density substrates. And, as always, OEMs are going to seek the lowest prices. The transition will be less traumatic for those manufacturers that have already invested in new technology, but will be difficult for those that have put off such investments. ○

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