

The recently published 1998 NEMI roadmap represents the combined work of over 400 industry experts from 175 companies and organizations in North America. Intended to identify the key technology and infrastructure developments required to ensure the competitiveness in electronics manufacturing, the roadmap looks at five product sectors and 17 technology areas. This article summarizes the chapter on organic interconnect.

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NEMI Roadmap

Points to Increasing Density of PWBs and Emergence of Microvia Technology

Introduction

The complex semiconductor devices and high-speed circuitry of today's electronics are dramatically changing the role of interconnection substrates. No longer does the substrate just provide a replacement for wire – it must match the characteristics of the electronic components being produced.

The interconnecting substrate provides circuit signal matching, thermal management, and mechanical support, as well as electrical functionality. These characteristics are no longer trivial. They are needed to support the advancements made in semiconductor technology that have occurred in the past decade and are continuing to evolve at a phenomenal rate. It is of little consequence to have semiconductor chips provide functions at speeds that are approaching the speed of light, unless these sophisticated devices can work together and talk to one another. For this to happen, electronic communication between the devices must occur economically and reliably. And the communication is dependent on both the placement of the components, the substrate materials used to make the interconnecting structure, and the multifaceted inter-relationship between these two.

As more of the circuit customization goes into silicon and the component package size increases, the printed board size will also change. With increased complexity comes increased I/O count and reduced contact pitch. Reduced contact pitch represents challenges for both assemblers and bare board

manufacturers. Assemblers have handling problems, coplanarity difficulties, and alignment problems. The board manufacturers have land size issues, solder mask difficulties, and electrical test problems.

Higher I/O demand will require multilayer or high density interconnection (microvia) designs to support the wiring needs for closely spaced devices, or to provide the escape routing from internal connections of array component. As the pitch changes, high density boards become mandatory and this means the boards become more difficult to produce.

In today's market, standard FR-4 represents 85% of the resin system used to produce copper clad laminate. These materials have been predominantly used to manufacture multilayer products. The characteristics of epoxy resin systems will continue to evolve. However, since the infrastructure is familiar with using epoxy laminates, the new resin developers are concentrating on enhancement of the characteris-

tics of epoxy, as opposed to looking at newer resin systems to provide the needs of the interconnecting structure.

All equipment manufacturers are looking at the packaging techniques for their products for the future. As these products become more complex and must meet more stringent consumer requirements, a measure of goodness in value as well as density is being developed.

Some of this relates to the number of physical components that the interconnecting structure must interconnect. Since interconnection is a major part of the characteristics, the input/output (I/O) of a component is an important issue.

Table 1 shows the projected interconnection needs of the five product sectors considered by the NEMI roadmap, plus a semiconductor super component (HDMB). For each of the five product sectors (which are standard among the NEMI, SIA and IPC roadmaps), a "product emulator" was developed and roadmap discussions are based

Table 1.

Product type	Maximum parts per cm ²	Maximum I/O per cm ²
Low Cost	20	62
Hand Held	33	140
Cost Performance	20	100
High Performance	35	90
Automotive (4 layer w/microvia)	17	12
Military (10 layer with blind or buried vias)	21	60
Super Component (8 layer; 35 mm ²)	0.16*	82

* Represents a single chip on a 25.4 mm substrate.

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on the projected characteristics of these emulators. The five product sectors are:

- Low cost – cameras, entertainment
- Hand held – cellular phones, sub-notebooks, PDAs
- Cost/performance – personal computers, servers, high-end games
- High performance – super computers, high-end workstations
- Harsh environment – auto under the hood, military, avionic electronics.

Table 1 has segmented the harsh environment market into two sections. In addition, a single chip interconnecting substrate has been added to reflect the need of the high density microcircuit board (HDMB).

There has been a dramatic increase in maximum component density (in parts per cm²), and maximum I/O density (in I/Os per cm²) in the last four years. The numbers shown in Table 1 reflect that increase.

Technology Issues

Technology requirements are different in each end use environment and are based on very specific functions that the interconnecting structure and assembly must perform. Table 2 shows examples of some of the low cost, readily available, high usage, copper clad laminates and their applications. Most of these are organic resin systems, which are supported by various reinforcements (most commonly glass fabric) to provide higher structural strength.

As can be seen from Table 2, the various applications cross over into different markets. Designers make tradeoffs and use the materials and their various properties, where appropriate, to serve the needs of a particular product.

As mentioned previously, the role of the interconnecting substrate continues to grow and may include functions such as impedance control or utilizing integral inductive/resistive/capacitive layers. In

addition, organic copper clad laminates have been targeted to replace the ceramic interconnecting structure inside large components, specifically plastic ball grid arrays (BGAs). Thus organic substrates must meet:

- the thermal and moisture-resistance profile for BGA parts, as required by the present standards;
- the precise edge definition, as required for manufacturing control;
- and precise dielectric thickness, for electrical performance.

The interconnecting and mounting structure will require greater precision in the placement and definition of the conductors and in the dielectric properties of the material. Moreover, the substrate used will likely require that the interconnecting structure already contain materials necessary for attachment of the components (e.g. solder bumps, palladium coated lands, conductive adhesive).

Table 3 represents the status

of technology in the interconnection industry for 1999. From this table it can be seen that 100 μm conductor (line) width and spaces on conventional FR-4 processes are available in limited production quantities, and 50 μm lines and spaces are available only from very select fabricators. Microvia technology is not used in conventional printed boards because products in those markets allow more liberal tolerances, since the products are rather simple and do not require high density wireability. Microvias today show up in threshold and state-of-the-art products, as exemplified by their use in high-end laptop computers and video recorders, and in special niche markets. These products are being produced with 75 μm lines and spaces.

Situation Analysis

Package Conductor Routing

Growth in the use of array type components such as BGAs and CSPs and direct attached flip chips is providing an increasing challenge to the interconnecting substrate manufacturer. Using high I/O components such as BGAs and CSPs creates the challenge of routing all the required signal, power, and ground I/O pins to the PWB without increasing PWB complexity and, therefore, cost. Thoughtful package pin assignments along with the package configuration considerations (pitch, ball size, ball count, and depopulation) can go a long way toward making the board routing easier.

For example, signal pin assignments need to be kept on the outer rows of an array package, using no more than four rows deep for all I/Os that need to be escaped. A 25 mm square BGA with a 1.25 mm pitch has a 19x19 ball matrix that has the ability to provide 361 I/Os. The outer four rows contain 240 pins; if a designer can work within these limits and still satisfy function, board routing can be easily accomplished by one conductor between lands for the two outer rows and Z axis escape for the lower ball count two inner signal rows (Rows 3 and 4). One conductor between lands routing is very cost effective,

Table 2. Copper Clad Laminate Applications.

Grade	Composition	General Properties	Applications	Comments
CEM-1	Epoxy/Glass Fabric Surface Epoxy/Cotton Paper Core	Punchable at room temperature Good electricals but less than polyester Good flex and impact strength	Consumer electronics	Good all-around laminate for punching Performance varies greatly between suppliers
CEM-3	Epoxy/Glass Fabric Surface Epoxy/Glass Paper Core	Punchable but harder than CEM-1 Good electricals Suitable for PTH applications	Computer peripherals Keyboards	One domestic source & difficult to obtain Popular in Far East for two-sided applications
FR-4	Epoxy/Glass Fabric	High flex & impact strength Excellent electrical properties Excellent for PTH applications	Computer applications Telecommunications Military	Most popular laminate material for drilled PTH applications
G-10	Epoxy/Glass Fabric Non Flame Retardant	High flex & impact strength Excellent electrical properties Excellent dimensional stability	Structural applications	Used as an unclad laminate for structural parts Non flame retardant
FR-5	Modified Epoxy/ Glass Fabric	Improved hot flex strength over FR-4 Excellent electricals	Military applications	Original FR-5 materials have disappeared Properties vary greatly between suppliers
Flex	Polyimide Polyester FEP	High flexibility High ductility copper Excellent electrical properties Excellent thermal properties	Computer applications Military applications Telecommunications Automotive	Polyimide is the most popular material
High Performance	Polyimide PTFE (Teflon®) Cyanate Ester Epoxy/PPE (Getek®)	Excellent thermal properties Lower x-y-z CTE High reliability Excellent electrical properties	High speed main frames Telecommunications Military	Polyimide is used in harsh environments, burn-in boards, down hole drilling, etc.

Note: PTH = plated through-holes

using 200 µm conductor width and 200 µm conductor spaces. In fact, two conductors between lands can be achieved on 1.25 mm grid using 150 µm and 150 µm lines and spaces at virtually no premium in cost. However, the total amount of real estate used may be higher and the performance may suffer slightly.

Technology Comparison

According to roadmap projections, the signal I/O count for the high performance market segment is about 2.5 times that for the hand held market segment. Note that the interconnection density requirement is linearly proportional to the signal I/O per package, and inversely proportional to the center-to-center pitch between the adjacent packages. A 2.5X increase in signal I/O from 500 to 1,300 pins per package at the same package-to-package pitch will require a PWB with a 2.5X increase in its wiring density, and a proportional increase in the density of the interlevel vias or plated through-holes (PTHs). This may require a reduction in the PTH pitch, and an increase in the number of signal layers in the PWB.

Table 4 is a summary of several characteristics of very high density microvia technology. It is not meant to be all-inclusive, but to act as an aid to fabricators and others in comparing technology alternatives. It is recognized that these technologies can be used to manufacture chip carriers (high density microcircuit boards) as well as planar boards. The row labeled "Conventional" in the following table is for comparative analysis.

Most of the techniques use a rigid four to six-layer FR-4 board as a core and build up a high density layer on a non-glass reinforced dielectric. The most promising ideas being evaluated in the U.S. include photovia technology and laser ablation. From a fabricator point of view, the photovia technology has the lead in infrastructure development. It is the most mature technology, and has products that are in the market, with proven reliability.

Table 3. Current State of Substrate Technology (Worldwide) – 1999.

	CONVENTIONAL Available from 85%		LEADING EDGE (Limited production) Available from 15% of the industry fabricators		STATE OF THE ART Available from less than 1% of industry fabricators	
	FR-4	Microvia	FR-4	Microvia	FR-4	Microvia
Line width/Line space	100 µm /100 µm	n/a	75 µm/75 µm	50 µm/100 µm	50 µm/50 µm	50 µm/50 µm
PTH hole size (un-plated)	350 µm	n/a	250 µm	100 µm	150 µm	50 µm
Drill capture land size	450 µm	n/a	350 µm	250 µm	300 µm	100 µm
Buried passive components	No	No	Very limited	No	Yes	No

Table 4 compares different microvia technologies with respect to capabilities, cost, versatility and other topics of common interest. The selected technologies have been expanded to include "hybrid lasers", a promising new development attracting considerable interest. It should be emphasized that these new hybrid laser machines are still being developed, thus the success of this technology is still to be determined. One could also make a case for distinguishing between CO₂ and TEA CO₂ lasers based on their different energy outputs and the resulting difference in economics. However, this was not attempted in Table 4.

The column identifying "hole diameter" of the microvias covers what is being built today and future capability. The quantification of this parameter can lead to misunderstandings. One should clearly distinguish between drilling capability and practical hole size limitations based on either the metallization process or a conformal mask imaging step. Lasers can create very small vias. Current copper plating techniques limit the practical application of these small vias. Furthermore, the aspect ratio of the hole for a given hole diameter needs to be stated. Dielectric type is a definition of the materials used for the microvia layer, and "layer count" is the number of micro-via layers that is practical. "Linear density potential" is a relative estimate of possible wiring density versus conventional technology. The potential linear density increases by the multiplier indicated as hole size decreases. Obviously, this multiplier is a rough estimate and makes the assumption that the hole can be plated.

Table 4 does not show land size requirements as they relate to different microvia technologies. Yet land size, more so than hole diameter, is a critical parameter which determines interconnect density limits, and is therefore mentioned here. One reason land size requirements were not included is the questionable informational value of a land size diameter without extensive specifications around substrate size, dimensional stability of the substrate, its thickness, and the aspect ratio of the via, to name a few. Furthermore, it is difficult to quantify the capture land and target land sizes required by the different microvia formation technologies. However, it is clear that the sidewall shape of the via will affect target and capture land sizes. Currently, target land to hole diameter ratios are in the neighborhood of 2:1, and it is expected that this ratio will increase as hole diameters shrink, unless thinner dielectric materials are used.

There is a direct correlation between the complexity (number of I/Os) of the electronic components and the I/O density (number per square centimeter). Leading edge printed board assemblies will be driven by the characteristics of the most complex/dense component and the package style of that part. It may be only one of a kind. The interconnection technology, however, must accommodate that part. The surrounding components may take advantage of the interconnect technology of choice, but it is not the driver toward the precision or capability of the processes used to make the interconnection. Electronic interconnections consist of conductors, spacing (planar & between layers) and the technology used to

create holes (through hole, blind via, buried via, etc.). Of all the interconnection methodologies, the manner in which holes are produced has the most effect on the relationship of the interconnecting structure and how it is produced.

Cost Expectations

The roadmap shows a projected cost comparison of different board configurations for both standard FR-4 boards and high density boards with microvias. The information provided represents the OEM expectations, but does not necessarily reflect the fabricator's ability to deliver. When designers interpolate their product to those characteristics shown for the six product sectors, they need to determine how close the fabrication can come to their expectations. In addition, the characteristics for a High Density Microcircuit Board, used to translate a bare die within a chip carrier from the die bonding pads to the array format of a BGA package style is shown.

Component Density and Wiring Complexity

Tables 6 and 7 show a component density comparison based on component usage for each of the product sectors. An evaluation is made between the maximum I/O and average I/O to help understand the relationship between these two characteristics and how that impacts the wiring complexity.

Table 7 provides a similar analysis except that here the ratio is based on the physical size of the parts. This parameter influences the fan-out requirement for various parts, thus showing the relationship of via location and test point access.

Table 4. Planar Board, High Density Micro-via Technology Comparison

Via Making Technology	Capital (equipment investment)	Adaptation to Existing Processes and Materials	Manufacturing Cost Blind/Buried	Blind Hole Diameter (not plated)	Dielectric Type	Build Up Dielectric Layer Count	Linear Density Potential
Conventional	Mechanical N. C. drills & conventional lamination presses	n/a	High: Z depth drilling. Moderate: for drilled cores. Little potential to go further	0.25 mm	All	Up to 50	1X
Photovia Liquid	Curtain coater or screening equipment. Planarizing equipment may be needed depending on hole size, dielectric overhang ("nose"), and compatibility of the dielectric surface with the metallization process. Improved expose/registration for multiple layers. Dedicated metallization line/process may be required	Moderate. Existing processes may have to be tailored and dedicated lines are preferred (see "capital")	High today. Will go lower with yield improvements and automation	Current: 0.09 mm Potential: 0.025 at 1:1 aspect ratio	Core is FR-4. Build up dielectrics are epoxy	Current is 4 layers per side; potential is >4 layers per side	2X
Photovia Film	Vacuum laminator. Improved expose/registration for multiple layers. Planarization not needed with low build-up layer count. May be needed with high layer count.	Moderate. Existing processes may have to be tailored and dedicated lines are preferred (see "capital")	High today. Will go lower with yield improvements and automation	Current: 0.100 mm Potential: 0.050 mm	Core is FR-4. Build up dielectrics are epoxy or epoxy blends	Current is 2 layers per side; potential is >2 layers per side	2X
Plasma	Plasma etcher and copper thinning (etch back) process	Good. Uses standard processes except for plasma etch. Copper thinning is an extra process. Suitable for flex substrates	Very high today with polyimide. Higher than photovia techniques with epoxy materials	Current: 0.100 mm Potential: 0.05 mm	Core is FR-4 or others. Build up can be a variety of organics, typically polyimide or epoxy, but not PTFE	Current: up to 2x; 8 layers bonded to a core construction	2X
Solid State UV YAG Laser	Laser drills	Very good. Laser can drill copper, glass, and resin simultaneously. Post-drill clean practiced to assure good copper-to-copper contact	Competitive. Higher via counts increase costs; but cost/hole is decreasing	Current: 0.03, but realistically 0.075 because of plating problem. Potential: 0.01 mm	All	>3 layers	3X
Gas CO2 Laser	Laser drills	Good. But requires copper pre-etch step. Requires post-drill clean (e.g. plasma) for electroless copper	Competitive. Higher via counts increase costs versus photo vias, but cost/hole is decreasing. Higher drill speed results in lower cost versus UV YAG laser	Current: 0.125 (difficult to image 0.075 mm diameter round copper mask holes) Potential: 0.05 mm	TEA CO2 can cut glass. New models of pulsed CO2 lasers can also cut glass	>3 layers	3X
Hybrid Gas CO2/Laser	Laser drills	Very good. Laser drills copper and resin sequentially in one drilling machine. Requires post-drill clean (e.g. plasma) for electroless copper	Competitive. Higher via counts increase costs; but cost/hole is decreasing. Japanese industry data indicates that higher drill speed results in lower cost versus UV YAG laser	Current: 0.03, but realistically 0.075 because of plating problems Solid State UV YAG Laser Potential: 0.01 mm	All	>3 layers	3X

Interconnection Substrate Materials

Many of the leading industry technology roadmaps (Semiconductor Industry Association, IPC, etc.) consider materials used in new technology applications to be the most important characteristic needed to meet the challenges of the twenty-first century. The materials form the basis of the interconnection, as well as the mounting structure for the electronic components in many of the products of the future. Consumer applications, particularly portable and telecommunications, are demanding that these laminates perform more functions than just interconnection. This includes high frequency applications with known dielectric constants and a control of the thickness requirement so that the manufacturing of the polymers provides electrical properties that are improved over the standard FR-4 materials. This is especially true for high-speed applications.

Traditional copper clad laminates have been used in the industry for many years to meet the requirements for mounting and interconnecting electronic components. Consumer applications, particularly portable and telecom, are demanding that these materials are produced as thin copper clad laminates to reduce size and weight. The emerging markets for PC cards and portable digital assistants will drive the need for thin, high performance interconnecting materials.

Frequency Drivers

As computers and modules reach processing speeds toward the 400 MHz level, signal speed and integrity become paramount. The high speed is mainly for the microprocessor. The interconnecting bus speed requirements are somewhat less, in the neighborhood of 100 MHz. The need for greater capability will be apparent as systems designed to be run above 200 MHz are still using FR-4, but the design becomes more difficult as frequency increases. As processing speeds continue to increase, pressure will continue to lower the dielectric constant and also lower the dissipation factor of the material.

Table 6 I/O Component Density Comparison.

I/O Component Density Comparisons	1999	2001	2003	2008
Low Cost (4 layer)	125/15=8.3	140/20=7.0	160/30=5.3	175/50=3.5
Hand Held (6 Layer, or 4 layer w/micro)	140/50=2.8	175/55=3.2	240/60=4.0	350/65=5.4
Cost Performance (4 layer)	100/10=10.0	100/12=8.3	150/13=11.5	225/22=10.2
High Perform. (14 layer, no blind/buried)	40/20=2.0	40/25=1.6	50/30=1.56	60/40=1.5
Automotive (4 layer w/microvia)	12/6=2.0	20/10=2.0	30/15=2.0	40/20=2.0
Military (4 layer w/microvia)	60/20=3.0	95/35=2.7	240/60=4.0	350/95=3.7
Super Component (single chip/daughter)	82/50=1.64	100/60=1.67	122/70=1.74	222/100=2.2

Note: The comparison table shows the relationship between the maximum component I/O and the average component I/O. A high percentage (i.e., 8.0, 5.4) signifies a greater amount of low I/O type components; a low percentage (i.e., 2.0, 1.6) signifies mostly high I/O count components.

Table 7 Component Part Density Comparison.

Component Part Density Comparisons	1999	2001	2003	2008
Low Cost (4 layer)	25/3.0=8.3	28/3.2=8.75	30/3.4=8.82	35/3.6=9.72
Hand Held (6 Layer, or 4 layer w/micro)	33/5.0=6.6	39/5.5=7.1	50/6.0=8.3	65/7.0=9.3
Cost Performance (4 layer)	20/1.0=20	30/1.05=28.6	40/1.1=36.4	75/1.25=60.0
High Performance (14 layer, no blind/buried)	35/1.5=23.3	60/2.6=23.1	110/3.0=36.7	205/3.5=58.6
Automotive (4 layer w/microvia)	17/1.8=9.4	28/2.1=13.3	37/2.6=14.2	56/3.2=17.5
Military (4 layer w/microvia)	21/2.3=9.1	32/2.4=13.3	38/2.5=15.2	47/2.6=18.1
Super Component (single chip/daughter)	0.16/0.26=.62	0.16/0.27=.59	0.16/0.28=.57	0.16/0.36=.44

Note: The comparison table shows the relationship between the maximum number of components per unit area compared to the average number of components. A high percentage (i.e., 23, 58) signifies a greater amount of small physical outline components; a low percentage (i.e., 3, 9) signifies mostly similar size components.

Advanced material technology is needed to provide robust solutions from a variety of polymer and carrier systems, which often utilize thermosetting polymers. For example, cyanate ester provides signal transmission speeds of 114 cm/nsec compared to 100 cm/nsec in normal FR-4 epoxy material. Lower dielectric constant (Dk) and lower dissipation factor (Df) provide the following solutions when selecting advanced material technologies.

Lower dielectric constant (Dk) benefits:

- Faster conductor signal speed
- Thinner interconnects for the same conductor geometries.

Lower dissipation factor (Df) benefits:

- Improved signal integrity with high frequencies
- Less signal loss at high frequencies.

Some of the newer materials evolving require characteristics that deal with not only their electrical properties, but also their mechanical properties. Since most NEMI emulator products are cost driven, their properties consider FR-4 as the

basic foundation. New formulations of epoxy resins are measured as to their price parity with the FR-4 market.

An attempt is being made by the industry to capture and enhance the benefits of epoxy resin systems with various reinforcements to address the industry needs. JEDEC committees responsible for the BGA package are approving and reviewing the material properties of epoxy reinforced resins. This enhances the mountability of the BGA since its coefficient of thermal expansion will be more in line with the CTE of the interconnecting substrate to which the component is mounted.

In today's market, standard FR-4 (multifunctional, tetrafunctional), represents 85% of the resin system used to produce copper clad laminate. These materials have been predominantly used to manufacture multilayer products. The characteristics of epoxy resin systems will continue to evolve. However, since the infrastructure is familiar with the use of epoxy laminates, the new resin developers are concentrating on enhancements to the characteristics of epoxy, as opposed to looking at

newer resin systems to provide the needs of the interconnecting structure.

Unreinforced Materials

When reviewing the material properties of various reinforced materials, one should not forget to examine unreinforced material properties, especially for high density boards. In some instances, new ideas are developing. Unreinforced laminate has been used for many years in flexible application. In these instances, the polyimide or polyester films are employed to provide thin material properties as well as high performance characteristics.

The main concern with unreinforced materials has been their dimensional stability. It is a well-known fact that the reinforcement provides some of the characteristics that impart CTE properties in the XY axis. This axis is the particular segment of the interconnecting product that affects the stress on the solder joints of the parts mounted on the interconnecting product.

It may be more advantageous to use non-reinforced materials. Although they are more flexible, they also provide less stress as the expan-

sion of the interconnecting substrate is different than that of the components mounted thereon. This characteristic may be a benefit rather than a detriment and many designers are exploring the use of combinations of reinforced and unreinforced materials.

There is a future need from a manufacturing perspective for ease of processing and consistency. Manufacturers of flexible products have found for years that their ability to predict the movement of the materials has greatly enhanced their capabilities in meeting customer requirements. Combinations of thin materials, unreinforced materials, and reinforced materials with high Tg or superior electrical properties will continue to evolve to meet the demands of the products of the twenty-first century. All of the issues can and are being addressed. The infrastructure needs to make decisions so that market share drives the cost of the selection to a minimal few and allows the producer of copper clad laminate, or its

equivalent, to be successful in meeting the demands of the industry.

Roadmap Conclusions

The roadmap lays out a number of conclusions relative to the future needs of the industry. A subset of these is provided in this section.

Critical Issues – Paradigm Shifts

A number of potential paradigm shifts could occur as a result of efforts to reach interconnection density targets under the expected cost constraints. These shifts, if they occur, will require new materials and processes beyond those in today's industry, e.g. FR-4 replacements.

One of the most significant paradigm shifts that may occur is a move to sequential boards. Increased wiring density for high I/O devices has uncovered limitations in the traditional printed board design and manufacturing techniques. High wiring density can be accommodated by increasing

layer count, or through densification using sequential manufacturing techniques (multilayer or double-sided) or fully additive.

Potential advantages of this type of construction can include very high wiring density through use of high density microvia technology plus reduced layer count and smaller boards.

Other possible paradigm shifts include:

- Deposited copper boards requiring:
 - new materials
 - significant capital investment
 - new control technologies
- Non-reinforced substrates
- Non-woven substrates

Gaps and Showstoppers

The major showstopper affecting the interconnect industry is the loss of captive R&D. In the Eighties, half of the printed board manufacturers were independent, the other half of the manufacturers were captive manufacturers. Today, most board

fabrication is out-sourced and a gap now exists for support of research in the printed wiring board area. The precipitous decline in substrate R&D investment does not bode well for meeting the ambitious emulator density and cost targets.

BIOGRAPHIES

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