Flip-Chip Technology In Organic Chip Carriers

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Advantages and growing pains.

Flip-chip technology has experienced a sharp increase in volumes across a wide range of applications in recent years. This trend is expected to continue and to accelerate over the next five years, with global consumption of flip-chip devices projected to exceed three billion devices by 2001. Current consumption is estimated at one billion, which is a significant increase from 1991 levels of about 250 million. This growth is reflective of a fundamental shift in technology from peripheral wiring to area-array interconnect wiring, driven, in part, by denser circuitry, higher frequencies and higher performance. Flip-chip devices are currently used in a wide range of applications, including computers, displays, hard drives, cell phones, automotive, medical and watches.

Flip-chip technology represents a major change in first-level packaging characteristics from traditional bonding technologies such as wire bonding. In flip-chip packages, the chip is mounted with the active side of the chip facing the chip carrier or substrate (Figure 1). The interconnections between the chip and the substrate consist of solder bumps that are about 0.003 to 0.005 in. in height and are typically located in an area array that may cover the entire surface of the chip.

Advantages, Characteristics

Flip-chip technology offers several advantages for many of today’s high-frequency, high-performance applications. It allows for area-array interconnections and also enables interconnections over active circuitry within the silicon, thus providing a relatively high number of interconnections. A flip chip is equivalent to a fully packaged chip in that it is sealed by the under-bump metallurgy and chip-passivation layer and provides an interconnection structure to the next-level package. A properly constructed flip chip mounted on a suitable carrier for interconnection, but with no other encapsulation, readily passes all the reliability requirements ascribed to a chip carrier.

Another significant advantage of flip chip is self-alignment. When the solder bumps reflow, the surface tension within the solder will self-correct for small misalignments of the chip. This self-alignment leads to extremely high manufacturing assembly yields. Flip-chip technology also offers low inductance, which is important for high-frequency applications.

Another important advantage of flip-chip technology is the ability to bring power into every quadrant of the chip. This ability provides uniform current distribution over the entire chip area as opposed to the peripheral distribution of wire bond, which requires bussing from the edge to the middle of the chip. This feature is particularly important in high-power applications. Flip chip also minimizes electromagnetic interference (EMI), which is a concern for RF (radio frequency) applications. Finally, flip chip can be a very low-cost interconnection technology due the elimination of the package and the potential for decreased chip size, which saves in the use of silicon.

A number of different configurations for the solder bumps and for the bounding layer of metallurgy on the silicon die itself exists. At

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IBM, a typical solder bump would have, starting from the silicon, an aluminum pad followed by 1,000 angstroms of chromium, 3,000 angstroms of chromium-copper, and 3,000 to 5,000 angstroms of copper. The solder would be delivered through evaporation. Lower cost technologies include plating, stud bump and stencil screening of solder paste. While this article will focus on packaging issues and characteristics, Reference 1 provides an excellent summary of the different solder bump technologies and bounding-layer metallurgies.

**Mechanical, Thermal Characteristics**

Flip-chip technology has been used extensively by IBM and others for more than 30 years. While the primary application has traditionally been in ceramic chip carriers, much of the recent growth has been in flip chip on less expensive organic carriers. This growth has become possible due to the availability of appropriate underfill materials to relieve the thermal stresses created by the large difference in thermal coefficient of expansion (CTE) between silicon and PWB materials. Ceramic and organic chip carriers have different characteristics and require different considerations in product design.

**Ceramic Chip Carriers**

Originally, flip chips on ceramic were used without an underfill. The primary mechanical concern under such conditions is the fatigue life of the solder, which is driven by the mismatch between silicon, with a CTE of about 3 parts per million (ppm), and alumina ceramic, with a CTE of approximately 6.5 ppm. As the package undergoes thermal cycling, the solder will experience shear stresses, resulting in eventual fatigue. Solder fatigue is a function of the distance from the neutral point (DNP) of the solder joints, typically the center of the chip. Fatigue life is degraded as the DNP increases. Typically, DNP is a function of chip size; therefore, using underfill to improve fatigue life has become necessary as chip sizes have increased over the years.

Underfills are basically high modulus materials with a CTE that is comparable to or lower than that of solder (20 to 30 ppm). The underfill should have very good adhesion to the silicon and the passivation layer on the chip, as well as to the substrate. The underfill can, then, reduce the shear stresses in the solder, thereby greatly improving fatigue life. The reduction in shear stress results in an increase in bending of the package which, in the case of ceramic packages, does not cause significant concerns. Reference 2 discusses the effect of underfill on flip-chip reliability in ceramic carriers in detail.

A concern of non-underfilled flip-chip technology on ceramic carriers is applying any significant mechanical load to the chip, which results in a transfer of the load to the solder bumps and, in turn, reduced fatigue life. This concern led to thermal management schemes that provided a good thermal path from the backside of the chip without putting a significant mechanical load on the chip itself. Examples of such thermal management include thermal grease and the IBM thermal conduction module, which has metal (aluminum or copper) pistons that apply a small and controlled compressive load to the chips. The advent of underfills reduced the concern about applying a load to the chip, and attaching a heat sink or heat spreader directly to the chip using thermal adhesives became possible (Figure 2). This attachment ability provided opportunities to reduce cost and to improve the thermal performance of the package. Overall, the mechanical and thermal behavior and reliability of ceramic flip-chip packages are fairly well understood, and solder fatigue life can be predicted with reasonable accuracy.

**Organic Chip Carriers**

With organic chip carriers the mechanical behavior of the package is substantially different and introduces a number of additional concerns. The CTE of typical organic chip carriers ranges from 15 to 20 ppm. The mismatch between the chip and chip carrier is, therefore, significantly larger than for ceramics, and using underfill for the majority of flip chip on organic applications is necessary. However, when underfills are used in organic chip carrier applications, high stresses and significant bending of the package may occur. These high stresses do not occur in wire-bond packages because the chip is not strongly coupled to the chip carrier as

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**FIGURE 2:** A flip-chip package with a heat sink attached directly to the chip. The heat sink changes the mechanical behavior of the package and, therefore, alters the reliability of the ball-grid array.

**FIGURE 3:** A typical wire-bond package showing the chip attached to the chip carrier via an adhesive layer. The chip and carrier do not need to be coupled mechanically as in flip-chip packages.
Flip-Chip Technology Projects: Advancing the State of the Art

Recognizing that underfills would be the norm in the future, both the Integrated Engineering Electronics Center (IEEC) at the T.J. Watson School of Engineering, State University of New York at Binghamton (Binghamton, NY), and the National Electronics Manufacturing Initiative (NEMI, Herndon, VA) have undertaken projects to advance the state of the art. The IEEC has a major DARPA-funded project underway to understand and model the flow process. Research at the IEEC has addressed the speed of the flow process, the development of models and the relationship to the material properties of the underfill. Currently, experimental and analytical work is being carried out to study void formation during the underfill process. The IEEC is also involved in several research projects dealing with solder fatigue, fundamentals of solder reflow and the reliability of organic chip carriers, particularly flip-chip and chip-scale technologies.

NEMI has focused its efforts on improvement of underfill materials. The consortium’s members have worked together to develop a commercially available underfill with a flow time of less than one minute, as compared to a typical 10- to 15-minute flow time. Current projects are centered around reducing cure times—from 60 to 90 minutes to five minutes or less—through development of new materials and/or new curing technologies. Over the long term, NEMI hopes to develop next-generation underfill materials that require minimum dispensing and no separate process step for curing.

For more information, contact the IEEC at (607) 777-4332 and NEMI at (703) 834-0330.

shown schematically in Figure 3. The major difference is that in the flip-chip package the coupling of the chip to the carrier is necessary for the reliability of the package. However, in the case of wire bonding, a thick layer of relatively low modulus adhesive may be used, thereby substantially decoupling the chip and chip carrier.

The stresses are first introduced into the package at the underfill cure stage. Typically, underfills may be cured at 120º to 165ºC, with the package at a low-stress condition at that temperature. However, as the temperature is reduced to room temperature, a significant residual stress builds up in the package. The module is then attached to the card, and the solder is frozen at around 220ºC. Finally, depending upon the application conditions, a heat sink may be attached to the chip or to the cover plate if one is used (Figure 2). The heat sink is mechanically coupled to the chip at the adhesive-cure temperature, which, in turn, changes the overall mechanical behavior of the package. The application may require single- or
double-sided module attach to the card, as shown schematically in Figure 4. With the advent of microvia boards and new underfill materials, flip chip migrating from ceramic to the lower cost organic chip carrier has become practical.

**Design for Manufacturing**

Flip chip on organic carriers is finding many new applications and can be a robust and reliable technology. However, understanding the design parameters and carrying out the appropriate reliability modeling is important. Understanding the design parameters and modeling the potential failure mechanisms can lead to robust structures and less time spent on rote testing, which ultimately leads to faster introduction to manufacturing.

The overall high residual stress in the package may cause any of the following problems:

* **Module Level**
  - Chip cracking: High stress and bending of the package may cause the chip to crack. Chip cracking may be observed as early as the cool down from the underfill cure process. Silicon cracking will occur when the stress in the package exceeds the silicon strength. Cracks may originate from surface or edge defects. Silicon strength may be improved by reducing dicing defects and by improving the surface condition of the wafers.
  - Delamination of the underfill from the chip-passivation layer: Delamination will occur when the stress at the interface exceeds the interfacial fracture strength. Surface preparation and a cleaning step may be required prior to underfill delivery. The use of a coupler to improve adhesion may also be necessary.
  - Delamination of the underfill from the solder mask on the chip carrier: Considerations are similar to those arising in delamination from the chip-passivation layer.
  - Delamination of the solder mask on the chip carrier: If the stress in the package exceeds the interfacial strength of the passivation to the chip-carrier resin, that interface will fail. Improving adhesion at the interface may be necessary.
  - Delamination of the passivation layer on the chip: This delamination is a rare occurrence and is usually associated with edge defects in the underfill such as a small or missing fillet.
  - Delamination of the thermal adhesive from the chip or cover plate: As with the solder mask, if the stress exceeds interfacial strength, delamination will occur. Surface cleaning and the use of couplers to improve adhesion may be necessary.
  - Fatigue fails of the signal traces and/or plated through holes in the chip carrier: These fatigue fails are application and design dependent.
  - Cracking of the underfill material: Cracking will occur if the stress in the material exceeds the fracture toughness of the material.

* **Card-Assembly Level**
  - Early fatigue of the ball-grid array (BGA): This fatigue will occur in thermal or power cycling due to the mismatch in CTE between the card and the module. Although the chip carrier alone is fairly well matched to the card, the module may be significantly different in effective CTE from the card after chip assembly and underfill cure. This problem may be exacerbated for double-sided appli-
cations (Figure 4). Under these circumstances the stresses in the BGA may be significantly higher since the card is not able to bend with either module due to symmetry.

- Delamination of the heat sink to the thermal adhesive interface: Considerations are similar to those for delamination of the cover plate.
- Delamination of the chip to thermal adhesive interface.

Conclusion

All of the concerns and difficulties outlined above for organic flip-chip packages can be eliminated or reduced through appropriate design and manufacturing practices. Designs should account for the increased stress due to the coupling between the chip and carrier, and analyses of the design should consider the exact nature of the application conditions and assembly configurations. Manufacturing processes should note the high stresses present in these packages, which result in very high sensitivity to contamination on any surface. Special cleaning techniques may be needed. Measurement techniques may be needed to evaluate interfacial strength and interfacial delamination. These considerations, inspections and measurements, and additional process steps may result in additional cost and, perhaps, lost yield. However, as different manufacturers and assembly houses increase their knowledge base, many of these concerns and inspections may be eliminated.

References


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