Board Assisted BIST: Long and Short Term Solutions for Testpoint Erosion – Reaching into the DfX toolbox

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Problem: 2009 iNEMI* Roadmap determined risk from manufacturing test-point elimination due to higher speeds and shrinking form factors.

Solution?: Can IC BIST* usage at Board level test to address this?
- Most “chip” level BISTs are designed for IC manufacturing,
- Tests and algorithms are often not optimized to run at board test,
- No standard chip level interfaces or algorithms,
  - Limits the introduction of BIST at board level test,

Project team to investigate:
- What is current adoption of IC BIST at board test?
- Which BISTs would be the most useful at board test?
- How can these be optimized or standardized?

* International Electronics Manufacturing Initiative
** Integrated Circuit Built In Self Test
What is iNEMI?

• International Electronic Manufacturing Initiative (iNEMI) is an industry-led consortium:
  – Electronics manufacturers, suppliers, industry associations,
  – Government agencies and universities.

• Members collectively:
  – anticipate future technology and business needs,
  – develop responses to meet those needs.

• Board and Systems Manufacturing Test Technology Integration Group (TIG) runs projects addressing test gaps.
  – related project “Structural Test of External Memories”
Outline of the Presentation

• Goal of BA-BIST project
• Value-adds of IC BIST at board level
• Phase 1 Survey
  – IC BIST current and future adoption at board test
• Phase 2 Survey
  – Use-case generation for standardization
• Phase 3 Scope
  – Standardization to drive industry standard changes
• Conclusions
Purpose of iNEMI’s BIST Project?

• Goals:
  – Develop and promote the adoption of IC BIST at the board/system level
  – Steer IC providers toward BIST functions helpful for board/system level test
  – Provide board level standardization requirements for BIST interfaces and algorithms
  – Encourage IC vendors and ATE/Instrument providers to provide standard products and tools based on these standards for BIST design.
What’s Driving IC BIST at Board Test

- Device geometry, pitch, pin-count following own Moore’s Law
  - ICT less capable to detect and isolate all manufacturing defects.
  - Micro via challenges for SerDes links above 3.4 Gb/s.
- High Density Interconnect (HDI) leading to lack of test-point access
- Board design, layout and manufacturing important part of overall product function
Phase 1 - Understanding Board Level IC BIST Adoption

- Team drew up survey with objective to obtain IC BIST adoption data:
  - Gauge how much component BIST is currently run at board level test.
  - Are there are any roadblocks to run it at board level?
  - Evaluate how useful it is for board level test.
  - Validate its future use for board level test.
  - Gather data on use of existing standards.
Survey Demographics

<table>
<thead>
<tr>
<th>Industry Segment</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>OEM Telecommunications</td>
<td>19%</td>
</tr>
<tr>
<td>Test Equipment</td>
<td>12%</td>
</tr>
<tr>
<td>OEM Semiconductors</td>
<td>10%</td>
</tr>
<tr>
<td>OEM Computer</td>
<td>9%</td>
</tr>
<tr>
<td>EMS</td>
<td>8%</td>
</tr>
<tr>
<td>Test Services</td>
<td>8%</td>
</tr>
<tr>
<td>OEM Medical</td>
<td>7%</td>
</tr>
<tr>
<td>OEM Automotive</td>
<td>5%</td>
</tr>
<tr>
<td>OEM Aerospace</td>
<td>4%</td>
</tr>
<tr>
<td>OEM Electronic Products</td>
<td>4%</td>
</tr>
<tr>
<td>Research Institute</td>
<td>4%</td>
</tr>
<tr>
<td>Components</td>
<td>3%</td>
</tr>
<tr>
<td>PCBs</td>
<td>3%</td>
</tr>
<tr>
<td>University</td>
<td>2%</td>
</tr>
<tr>
<td>Government Agency</td>
<td>1%</td>
</tr>
<tr>
<td>OEM Marine</td>
<td>1%</td>
</tr>
<tr>
<td>OEM Military</td>
<td>1%</td>
</tr>
<tr>
<td>OEM Video Products</td>
<td>1%</td>
</tr>
<tr>
<td>Packaging Services</td>
<td>1%</td>
</tr>
</tbody>
</table>
IC BIST Available - Board Level

- IC external memory BIST: 92%
- Voltage monitoring: 97%
- Temperature monitoring: 100%
- Protocol-based functional BIST: 100%
- Electronic chip ID (die ID): 90%
- High speed I/O BIST or SerDes: 89%
- IC interconnection I/O BIST: 85%
- IC internal memory BIST: 97%
- Analog and mixed signal BIST: 84%
- IC logic BIST: 77%
- BIT error rate testing: 73%
- End Users - % ICs with test, where test can run at board level:
  - IC external memory BIST: 85%
  - Voltage monitoring: 80%
  - Temperature monitoring: 76%
  - Protocol-based functional BIST: 70%
  - Electronic chip ID (die ID): 70%
  - High speed I/O BIST or SerDes: 68%
  - IC interconnection I/O BIST: 62%
  - IC internal memory BIST: 57%
  - Analog and mixed signal BIST: 57%
  - IC logic BIST: 56%
  - BIT error rate testing: 45%

IC designers - % ICs with test, where test can run at board level:
- IC external memory BIST: 92%
- Voltage monitoring: 97%
- Temperature monitoring: 100%
- Protocol-based functional BIST: 100%
- Electronic chip ID (die ID): 90%
- High speed I/O BIST or SerDes: 89%
- IC interconnection I/O BIST: 85%
- IC internal memory BIST: 97%
- Analog and mixed signal BIST: 84%
- IC logic BIST: 77%
- BIT error rate testing: 73%

Legend:
- Green: End Users - % ICs with test, where test can run at board level
- Pink: IC designers - % ICs with test, where test can run at board level
Many IC BISTs are available and run at board level
- Internal & external memory tests, V & T monitors, IOBIST, Logic BIST are most popular
- 60% Board designers are requesting access to IC BIST.

Access to BIST is predominantly via IEEE1149.1 TAP

The majority of BIST tests are proprietary
- Potential roadblock to wider adoption and implementation

BIST run at the board level is good at catching defects

Currently run at many different board/system test steps
- Future use is more BIST during in-field maintenance, diagnostics and PCBA repair test.
Phase 1 Survey Key Takeaways

• However, some issues encountered:
  – Some ICs do not support BIST function,
  – IC suppliers often do not give BIST function to board users,
  – Lack of access when IC is mounted on the board,
  – BIST function at board test not supported by a standard.

• Looking to the future:
  – Seen to be critical for future fault isolation,
  – Would like BIST coverage to be > 80% at board test
  – > 75% respondents see BIST coupled with boundary-scan replacing lack of test point access.
  – > 50% respondents plan to adopt or are actively considering adopting current IEEE standards.
Phase 2 - IC BIST Use-Case Identification

- Phase 2 Survey Objectives:
  - Investigate and identify IC BIST Use Case to be used as standardization example for board and system applications
  - Get board/system test/debug engineers to identify what their problems are, and what may be solved with a “BIST function”
  - Definition of IC BIST to be used for Board/System purposes
  - See if board test solution needs align with solution IC designers are providing
  - Identify Users of BIST (NPI, BT, BD&Y, RMA)
  - Identification of BIST value-adds
Most Significant Problems Today

1st problem
2nd problem
3rd problem

- Loss of testpoint access or loss of ICT
- Debugging diagnosing board failures
- Characterizing or testing high-speed traces
- Conducting failure analysis of failing boards
- Testing functionality of on-board chips
- Testing or dealing with high-speed (e.g.,)
- Structurally testing on-board memories
- Testing specifications of on-board chips
- Conducting PCOLA on chips on the board

Phase 2
Board-Assistance BIST is an embedded capability within an IC that is fully or partially self-contained, in that it incorporates some or all of the following capabilities: pattern/signal generation, pattern/signal delivery, response or data capture, and response evaluation functions.
How can BA-BIST Solve Your Problem today

- By providing a feature that can FAM test the interconnect between two chips on a board
- By providing a feature that can SOQ test the interconnect between two chips on a board
- By providing a feature that can provide PCOLA for the chip the BIST feature resides within
- By providing a feature that can provide PCOLA for other chips on the board
- By providing a feature that can provide a FAM test for the chip the BIST feature resides within
- By providing a feature that can provide a FAM test for other chips on the board
- By providing a feature that can test the memory within the chip the BIST feature resides within
- By providing a feature that can test the memory on other chips on the board

1st problem to solve
2nd problem to solve
3rd problem to solve
What Type of BA-BIST Solve Your Problem Today?

“What BIST functions board test wants or needs” AND

“What BIST functions IC providers support” agree on top areas for BIST needs:

• Memory BIST in the chip to test memories attached to the chip
• Digital Pattern Generators to drive data off chip through general purpose IO
• SerDes BIST (HSIO-BIST) to provide patterns to/through the PHY of the chip
• Memory BIST (MBIST) to test embedded memories within the chip
Test Environments Where Most Issues Occur

- Manufacturing board test
- New product introduction
- Board debug and diagnosis
- Field return evaluation
- Board yield analysis
- Other

1st problem area
2nd problem area
3rd problem area
Phase 2 Survey Key Takeaways

- BA-BIST needs to solve loss of test point access and SOQ-FAM* interconnect between 2 chips
- IC BIST functions map onto BA-BISTs needed by board test community.
- Main areas where BA-BIST functions are used:
  - Manufacturing board test, NPI, board debug and diagnosis.
- IC BISTs map onto same ROI factors for IC and Board Test:
  - Reduce test time, cost, external test equipment.

* Short, Open, Quality, Feature, At-speed, Measure
Phase 3 Use Case Standardization

• Phase 3 Goal to “standardize” BA-BIST on two use-cases:
  – HSIO (chip to chip)
  – ASIC to external memory

• Short Term Plan
  – Present to 3-5 years

• Long Term Plan
  – 3-5 years onwards
Short Term and Long Term Goals

• **Short Term**
  - Directed to today’s IC BIST
  - Reach out to top IC Suppliers to communicate value-add of BA BIST solutions
  - Request for BA-BIST and support tools

• **Long Term**
  - Develop tasks and tests for standardization
  - Logic and features
  - Access, control (initialization, tuning), configuration
  - Description and vectors
  - Standardization support statements in relation to existing IEEE standards

Now to 3-5 year

Implementation beyond 3-5 years
# Targeted Defects form Standards Base

<table>
<thead>
<tr>
<th>Fault Model Category</th>
<th>Test Type</th>
<th>Use Environment</th>
<th>Defect Classes</th>
<th>BA-BIST?</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trace Stuck-at-1,0</td>
<td>ICT, bscan</td>
<td>NPI, mfg test, debug, yield</td>
<td>Signal trace shorted/open to power/GND, Bridged to signal</td>
<td>yes</td>
</tr>
<tr>
<td>Trace transitions randomly</td>
<td>ICT, bscan</td>
<td>NPI, mfg test, debug, yield</td>
<td>Broken trace, open trace, undriven open</td>
<td>yes</td>
</tr>
<tr>
<td>Trace impedance</td>
<td>ICT, bscan</td>
<td>Mfg test</td>
<td>Malformed trace</td>
<td>no</td>
</tr>
<tr>
<td>High speed trace spec</td>
<td>At-speed func</td>
<td>NPI, debug, yield</td>
<td>Chip drive, malformed trace</td>
<td>yes</td>
</tr>
<tr>
<td>Signal integrity</td>
<td>At-speed func</td>
<td>NPI, debug, yield</td>
<td>Malformed traces</td>
<td>yes</td>
</tr>
</tbody>
</table>
Use case 1 - HSIO

- Connection of BA-BIST function to chip pins allows board test control, configuration, and access using P1687 Embedded Instrument Interface, described by ICL and PDL, connected through a compliant JTAG TAP.
Use case 2 - IC to External Memory
Conclusion

• Industry looking to BA-BIST to replace lack of test points at ICT.

• BIST already well adopted AND industry wants BIST board coverage to increase in future to 80%;
  – Want to SOQ and FAM interfaces chip to chip,
  – But IC BIST often not given out.
  – No standards for board BIST implementation

• Short term plan to increase industry awareness.

• Long term goal to provide BA-BIST standardization statements to relevant IEEE standard.