Bill Bader, iNEMI
iNEMI PCB/Laminate Workshop, Taipei
October 22, 2013
Agenda

• iNEMI Roadmap Process and Scope
• 2013 PCB Roadmap and TIG Outcomes
• Summary & Conclusion
2013 Roadmap

- > 650 participants
- > 350 companies/organizations
- 18 countries from 4 continents
- 20 Technology Working Groups (TWGs)
- 6 Product Emulator Groups (PEGs)
- > 8 Man Years of Development Time
- > 1900 pages of information
- Roadmaps the needs for 2013-2023
Collaboration With Other Organizations
Collaboration on Roadmapping

- iNEMI / ITRS / MIG / PSMA Packaging TWG
- iNEMI / MIG / ITRS MEMS TWG
- iNEMI / IPC / EIPC / TPCA Organic PWB TWG
- iNEMI Passives TWG
- iNEMI Board Assembly TWG
- iNEMI Optoelectronics TWG
- iNEMI Information Management TWG
- iNEMI Mass Data Storage TWG

- Organic Printed Circuit Boards
- Supply Chain Management
- Magnetic and Optical Storage
- Interconnect Substrates—Ceramic
- Semiconductors

- iNEMI / IPC / EIPC / TPCA
- Supply Chain Council
- iNEMI / ITRS / MIG / PSMA
- Optoelectronics and Optical Storage

- iNEMI / ITRS
- MEMS TWG

- iNEMI
- Optoelectronics TWG

- IEEE
- CPMT
- Surface Mount Technology Association
- Electronic Components Industry Association
- Microphotonics Center
- Taiwan Printed Circuit Association
Industry Led Teams

- **Technical Working Group Teams**
  - Develops the roadmap technology chapters
  - Presently 20 Teams and Chapters

- **Product Emulator Group Teams**
  - “Virtual Product”: future product attributes plus key cost and density drivers – Presently 6 Teams and Chapters
    - Portable / Consumer
    - Office Systems
    - High-End Systems
    - Medical Products
    - Automotive
    - Aerospace/Defense
iNEMI Methodology

Technology Roadmap Process
ID key market trends & Evolution
Potential disruptive technologies
Looking 10 years into the future

Further Refine Opportunities
Use technology working groups
Use organized workshops
To ID collaborative projects

Critical Analysis of Roadmap
Extract key gaps and challenges
Both Short & Long Term

Organize & Direct Projects
Teams formed to clearly identify scope/deliverables
Call for member participation
Manage collaborative R&D process
Ensure delivered results
Roadmap Technology Chapters

- Organic PCB
- Solid State Illumination
- Large Area, Flexible Elect.
- Semiconductor Technology
- Photovoltaics
- Ceramic Substrates

- Connectors
- MEMS / Sensors
- Packaging & Component Substrates

- RF Component & Subsystem
- Passive Components
- Optoelectronics

- Thermal management
- Environmentally Sustainable Electronics
- Modeling, Simulation, Design
- Information Management Systems

- Mass Storage (Magnetic & Optical)
- Energy Storage & Conversion System

- Board Assembly -> Final Assembly -> Test, Inspection, & Measurement

Green = Engineering  Purple = Manufacturing  Blue = Component & Subsystem
## Roadmap Development

### Product Sector Needs vs. Technology Evolution

<table>
<thead>
<tr>
<th>Product Emulator Groups</th>
<th>TWGs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Portable / Consumer</td>
<td><strong>Semiconductor Technology</strong></td>
</tr>
<tr>
<td>Office Systems</td>
<td><strong>Business Processes</strong></td>
</tr>
<tr>
<td>High-End (e.g. netcom, server)</td>
<td><strong>Design Technologies</strong></td>
</tr>
<tr>
<td>Automotive</td>
<td><strong>Manufacturing Technologies</strong></td>
</tr>
<tr>
<td>Medical Products</td>
<td><strong>Comp./Subsyst. Technologies</strong></td>
</tr>
<tr>
<td>Defense and Aerospace</td>
<td><strong>Packaging, Substrates, Displays, etc.</strong></td>
</tr>
</tbody>
</table>
Technical Plan for Members
5 Year Plan for Implementation

• Implementation Plan for Key Areas
  • Areas selected by TC
  • Plans developed and Prioritized by Members
• 2013 Plan Covers 8 Project Areas
• **Scope:** The Organic PCB TIG’s primary objectives are to provide substrate materials, processes, and equipment that enable cost effective, reliable bare PCB innovation in a global manufacturing environment.

• The TIG has identified gaps and issues that are a barrier to designing and manufacturing cost effective and reliable PCB substrates.
## Organic PCB Gap Analysis

<table>
<thead>
<tr>
<th>Performance</th>
<th>2013</th>
<th>2015</th>
<th>2017</th>
<th>2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Development of improved signal integrity performance PCB laminates</td>
<td>🟠🟠🟠</td>
<td>🟠🟠🟠</td>
<td>🟠🟠🟠</td>
<td>🟠🟠🟠</td>
</tr>
<tr>
<td>Smooth copper traces with improved adhesion to dielectrics</td>
<td>🟠🟠🟠</td>
<td>🟠🟠🟠</td>
<td>🟠🟠🟠</td>
<td>🟠🟠🟠</td>
</tr>
<tr>
<td>Cost effective high performance laminates for broader applications</td>
<td>🟠🟠🟠</td>
<td>🟠🟠🟠</td>
<td>🟠🟠🟠</td>
<td>🟠🟠🟠</td>
</tr>
<tr>
<td>driven by bandwidth miniaturization and cost (low Dk dielectrics for HDI)</td>
<td>🟠黄色</td>
<td>🟠黄色</td>
<td>🟠黄色</td>
<td>🟠黄色</td>
</tr>
<tr>
<td>Incident impedance and measurement of functional nets</td>
<td>🟠黄色</td>
<td>🟠黄色</td>
<td>🟠黄色</td>
<td>🟠黄色</td>
</tr>
</tbody>
</table>

### Alignment

| Drill to pad registration for tight pad stack requirements                  | 🟠黄色 | 🟠黄色 | 🟠黄色 | 🟠黄色 |
| Cost effective control of layer to layer registration                      | 🟠黄色 | 🟠黄色 | 🟠黄色 | 🟠黄色 |
| Reduction in max stub length for high aspect ratio backdrilling             | 🟠黄色 | 🟠黄色 | 🟠黄色 | 🟠黄色 |

### CAF

| Effect of lower resin content prepregs on CAF performance                    | 🟠黄色 | 🟠黄色 | 🟠黄色 | 🟠黄色 |
| Develop a stack-up design method and model to account for CAF risk          | 🟠黄色 | 🟠黄色 | 🟠黄色 | 🟠黄色 |

### OTHER

| Low cost flex and rigid flex options                                        | 🟠黄色 | 🟠黄色 | 🟠黄色 | 🟠黄色 |
| New non-contact testing techniques and cost effective electrical test methods| 🟠黄色 | 🟠黄色 | 🟠黄色 | 🟠黄色 |
| Cost models for optical interconnect vs. copper                            | 🟠黄色 | 🟠黄色 | 🟠黄色 | 🟠黄色 |
| Need for light optical interconnect standards                              | 🟠黄色 | 🟠黄色 | 🟠黄色 | 🟠黄色 |

*Manufacturable solutions exist, and are being optimized*

*Manufacturable solutions are known*

*Interim solutions are known*

*Manufacturable solutions are NOT known*
<table>
<thead>
<tr>
<th>Other</th>
<th>2013</th>
<th>2015</th>
<th>2017</th>
<th>2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low cost flex and rigid flex options</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cost effective electrical test of high interconnect PCBs</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Moisture effects on laminate properties</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCB Modeling (Warpage &amp; Performance)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Improved printed electronic inks and performance</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Evolving requirements for soldermask for new applications. Solder mask is becoming more of a structural element with underfill and corner glue</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known
## PCB 5 Year Plan

### Organic PCB 5 Year Plan

<table>
<thead>
<tr>
<th>Attributes</th>
<th>PCB (um)</th>
<th>HDI (um)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L/S</td>
<td>85/125</td>
<td>50/50</td>
</tr>
<tr>
<td>PTH / Pad</td>
<td>200/450</td>
<td></td>
</tr>
<tr>
<td>uVia/Pad</td>
<td>100</td>
<td>75/200</td>
</tr>
<tr>
<td>Z-Axis CTE</td>
<td>&lt;3% (25-260 C)</td>
<td></td>
</tr>
</tbody>
</table>

### Deployed Technology
- EP test (Resistors & Capacitors)
- Improved material Dk/DF
- Single pass filled uvia plating
- Halogen Free laminates

### Development
- Drill to padstack registration
- Improved signal to ref. layer reg.
- High density PCB electrical test
- Moisture effects on laminate prop.
- Reduction in backdrill stub length
- CAF perf. Of lower RC% prepreg
- Evolving requirements for SM

### Research
- Improved SI performance material
- Profile free copper traces
- Stackup model for CAF Risk
- Incident impedance measurement
- Conductive Ink Development
- Low Dk dielectrics for HDI
- Cost effective polyimide
- Laminate datasheet characteristics

<table>
<thead>
<tr>
<th>Attributes</th>
<th>PCB (um)</th>
<th>HDI (um)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L/S</td>
<td>75/100</td>
<td>40/40</td>
</tr>
<tr>
<td>PTH / Pad</td>
<td>180/380</td>
<td></td>
</tr>
<tr>
<td>uVia</td>
<td>80</td>
<td>70/160</td>
</tr>
<tr>
<td>Z-Axis CTE</td>
<td>&lt;2.8% (25-260 C)</td>
<td></td>
</tr>
</tbody>
</table>

### Deployed Technology
- Drill to padstack registration
- Improved signal to ref. layer reg.
- High density PCB electrical test
- Reduction in backdrill stub length
- Evolving requirements for SM

### Development
- Improved SI performance material
- Profile free copper traces
- Stackup model for CAF Risk
- Incident impedance measurement
- Conductive Ink Development
- Low Dk dielectrics for HDI
- Cost effective polyimide
- Laminate datasheet characteristics

### Research
- High performance laminates
- Cost effective HDI matl's/Process
- Incident impedance measurement
- Conductive Ink Development
- Non-solder based interconnects

<table>
<thead>
<tr>
<th>Attributes</th>
<th>PCB (um)</th>
<th>HDI (um)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L/S</td>
<td>66/88</td>
<td>30/30</td>
</tr>
<tr>
<td>PTH / Pad</td>
<td>150/375</td>
<td></td>
</tr>
<tr>
<td>uVia</td>
<td>80</td>
<td>60/150</td>
</tr>
<tr>
<td>X/Y-Axis CTE</td>
<td>&lt;10 ppm C (&lt;Tg)</td>
<td></td>
</tr>
</tbody>
</table>

### Deployed Technology
- Improved SI performance material
- Profile free copper traces
- Stackup model for CAF Risk
- Incident impedance measurement
- Conductive Ink Development
- Low Dk dielectrics for HDI
- Laminate datasheet characteristics

### Development
- PCB Modeling: Warpage/Reliability
- Non-contact testing techniques
- Cost effective polyimide
- Lite optical interconnect standards
- Cost model for optical interconnect
- Low cost flex/rigid flex

### Research
- High performance laminates
- Cost effective HDI matl's/Process
- Improved component embedding

### Attributes
- **2013**
  - L/S: 85/125
  - PTH / Pad: 200/450
  - uVia/Pad: 100
  - Z-Axis CTE: <3% (25-260 C)

- **2015**
  - L/S: 75/100
  - PTH / Pad: 180/380
  - uVia: 80
  - Z-Axis CTE: <2.8% (25-260 C)

- **2017**
  - L/S: 66/88
  - PTH / Pad: 150/375
  - uVia: 80
  - X/Y-Axis CTE: <10 ppm C (<Tg)

- **2019**
  - L/S: 66/88
  - PTH / Pad: 150/375
  - uVia: 80
  - X/Y-Axis CTE: <10 ppm C (<Tg)
## Long Term R&D Need

<table>
<thead>
<tr>
<th>&gt; 5 Years (Strategic) Gaps/Needs</th>
</tr>
</thead>
<tbody>
<tr>
<td>High performance laminates</td>
</tr>
<tr>
<td>Cost effective, improved performance, single lamination HDI buildup materials and processes</td>
</tr>
<tr>
<td>Radical Reduction in PCB Cost</td>
</tr>
<tr>
<td>New non-contact testing techniques</td>
</tr>
<tr>
<td>Optical waveguide technology: Laminated and embedded wave guides</td>
</tr>
<tr>
<td>Cost models for optical interconnect vs. copper</td>
</tr>
<tr>
<td>Need for lite optical interconnect standards</td>
</tr>
<tr>
<td>Lack of confidence in Laminate Datasheet Characteristics</td>
</tr>
<tr>
<td>Aging and long term effects on laminate resins</td>
</tr>
<tr>
<td>Cost Effective Polyimide</td>
</tr>
<tr>
<td>Non solder based interconnect technology</td>
</tr>
<tr>
<td>Improved components embedding process</td>
</tr>
</tbody>
</table>
What has changed

• Increased cost pressure from product sector emulators continues to be a major challenge, particularly as design complexity increases
• Increasing interconnect density as it becomes necessary to pack more function into smaller packages
• Higher performance demands driven by increasing buss speeds, increasing broadband network usage, data intensive analytics, and high definition images
• Ability of copper to support higher frequencies has further delayed the adaption of optical packaging solutions
  – Advancements in laminate performance and copper roughness profile for standard PCB packaging solutions
  – Immaturity of optical packaging technology & mfg processes
  – Cost prohibitive & high risk
www.inemi.org

Email contacts:
Chuck Richardson
chuck.richardson@inemi.org
Bob Pfahl
bob.pfahl@inemi.org