



International Electronics Manufacturing Initiative

# System in Package Technology

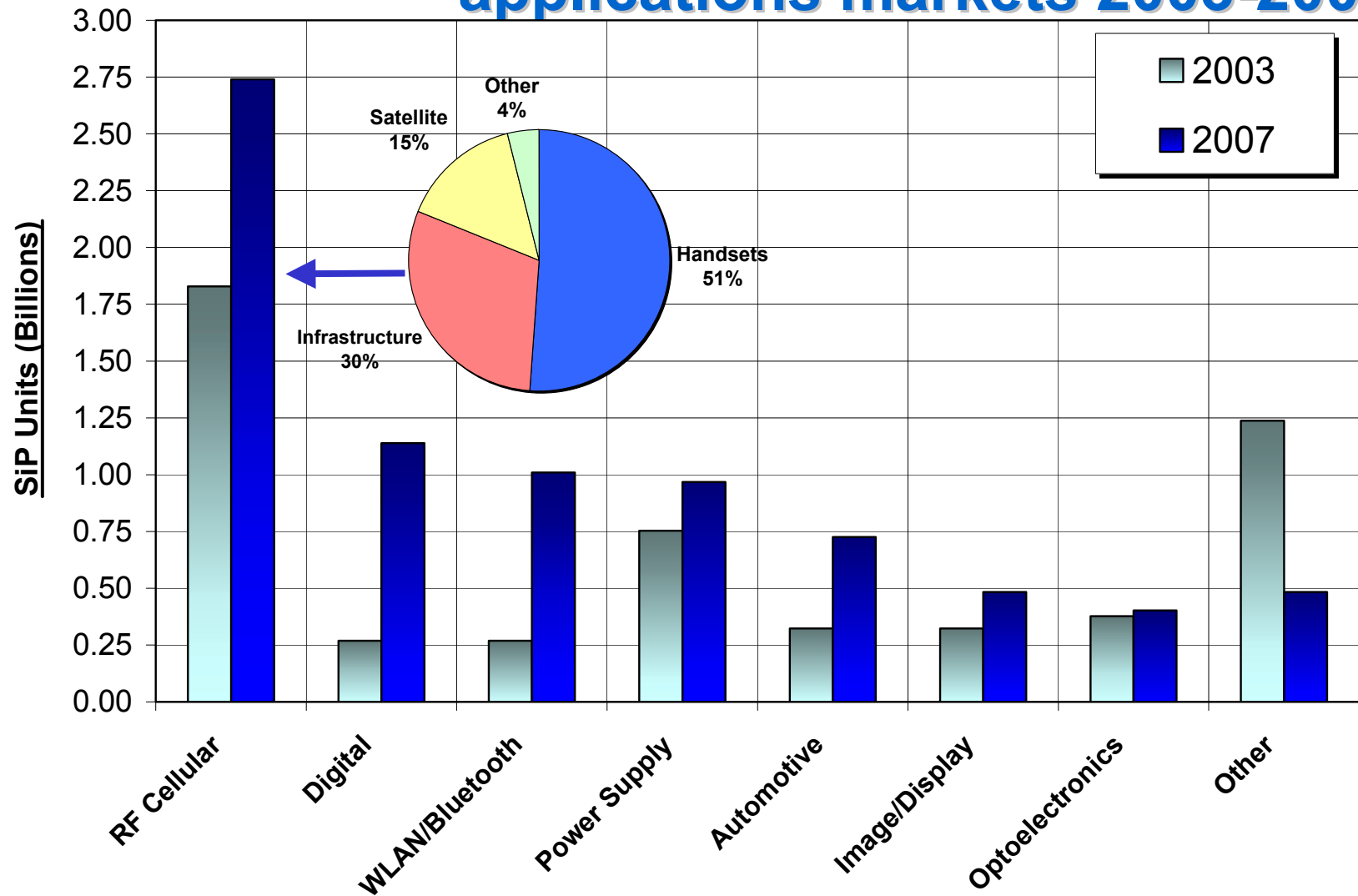


*Dr. Robert C. Pfahl, Jr., iNEMI*  
*Joe Adam, Skyworks*

- **Introduction**
- **iNEMI SiP Roadmap**
- **iNEMI SiP Technical Plan**
  - **Gap Analysis**
  - **Project Proposal**
- **Conclusion**

- **Volume drivers have shifted to consumer electronics**
- **Longer term growth will be driven by machine to machine**
- **System In Package has become a mainstream technology**
- **Chip Scale Packages are beginning to replace older leadframe technologies due to cost, size, and performance advantages**
- **Wafer level packaging technologies are taking off**
- **The contract assembly and test business has started to consolidate driven by a more competitive environment**
- **The EMS and Assembly and Test overlaps are increasing**
- **Improvements in cost are not keeping pace with pricing pressure**

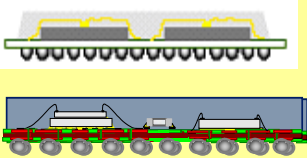
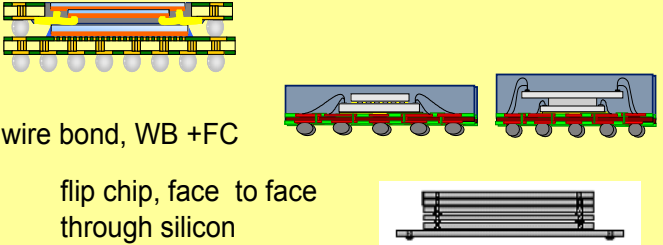
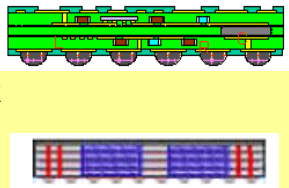
# Projected growth for SiP in key applications markets 2003-2007



Sources: Prismark (primary), Deutch Bank, Credit Suisse First Boston, Allied Business Intelligence.

## Definition for System-in-Package

*“System in Package is characterized by any combination of more than one active electronic component of different functionality plus optionally passives and other devices like MEMS or optical components assembled preferred into a single standard package that provides multiple functions associated with a system or sub-system.”*

Chip / Component Configuration	Technology	
<p>Side by Side Placement</p>	<p><b>Substrate:</b> organic laminate, ceramic, glas, silicon, leadframe</p> <p><b>Chip Interconnection:</b> wire bond and/or flip chip</p> <p>+ passive components</p>	 <p>integrated into the substrate discrete (CSP, SMD)</p>
<p>Stacked Structure</p>	<p>PoP   PiP</p> <p>stacked die</p> <p>chip to chip / wafer</p> <p>wire bond, WB +FC</p> <p>flip chip, face to face through silicon</p> <p>WL 3D stack</p> <p>wafer to wafer (W2W)</p>	
<p>Embedded Structure</p>	<p>Chip in PCB / polymer</p> <p>WL thin chip integration</p> <p>single layer</p> <p>multi-layer 3D stack</p> <p>single layer</p> <p>stacked functional layers</p>	



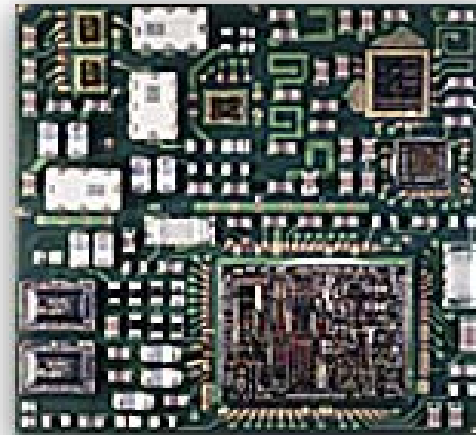
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# System in Package Roadmap



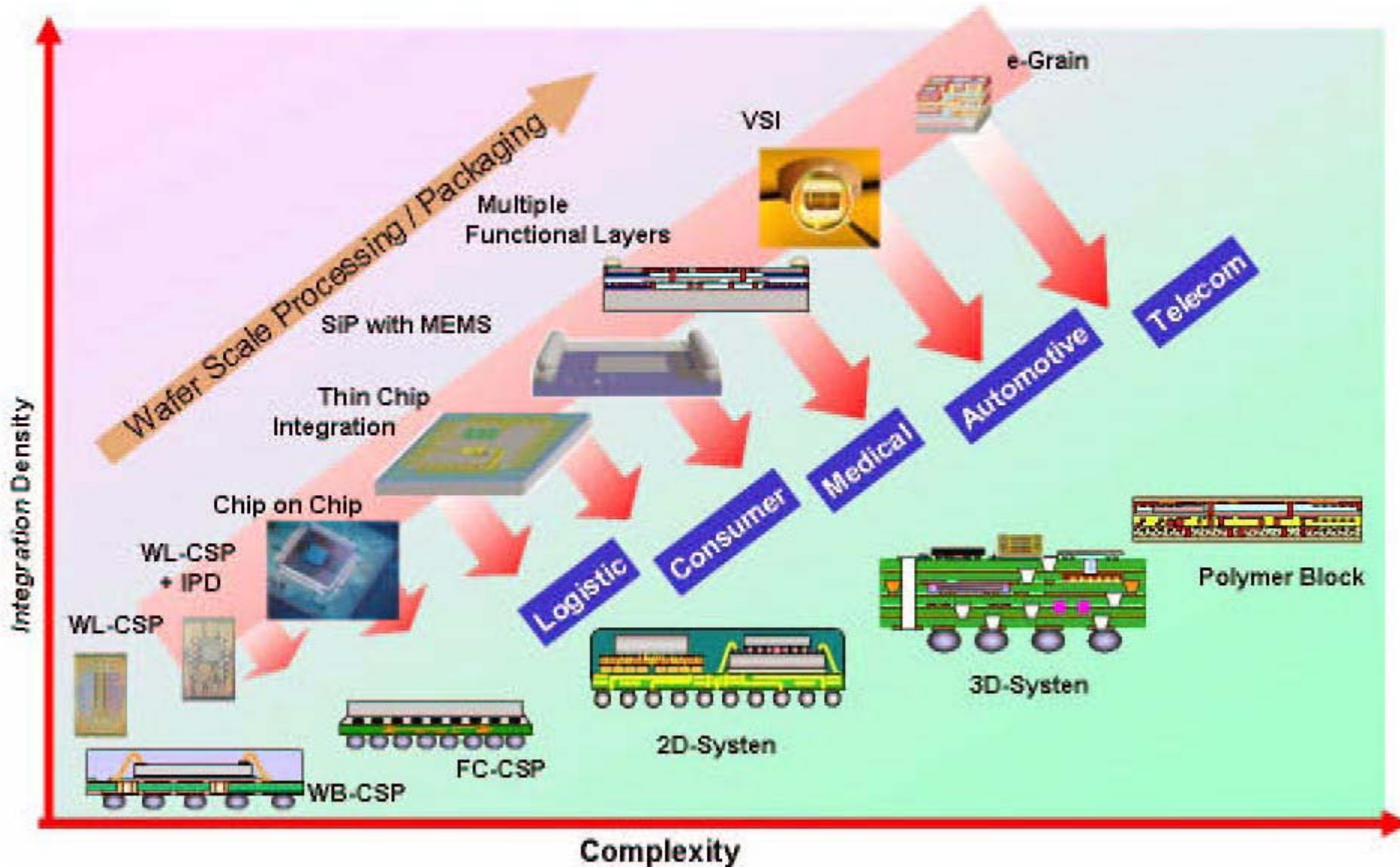
- **Broadest adoption of SiP has been for stacked memory/logic devices and small modules (used to integrate mixed signal devices and passives) for mobile phone applications**
- **SiP provides more integration flexibility, faster time to market, lower R&D cost, and lower product cost (for some applications) than SOC.**
- **Infrastructure issues facing SiP implementations include:**
  - **Need for low cost higher density substrates**
  - **High speed simulation tools for electrical & mechanical analysis**
  - **Lower cost Wafer Level Packaging**
  - **Lower cost Assembly Equipment**
  - **Lower cost improved materials for encapsulation**
  - **Skill set and business models vary for EMS/SAS**

# **iNEMI** Example of a module based SiP with radio functions for a GSM mobile phone radio

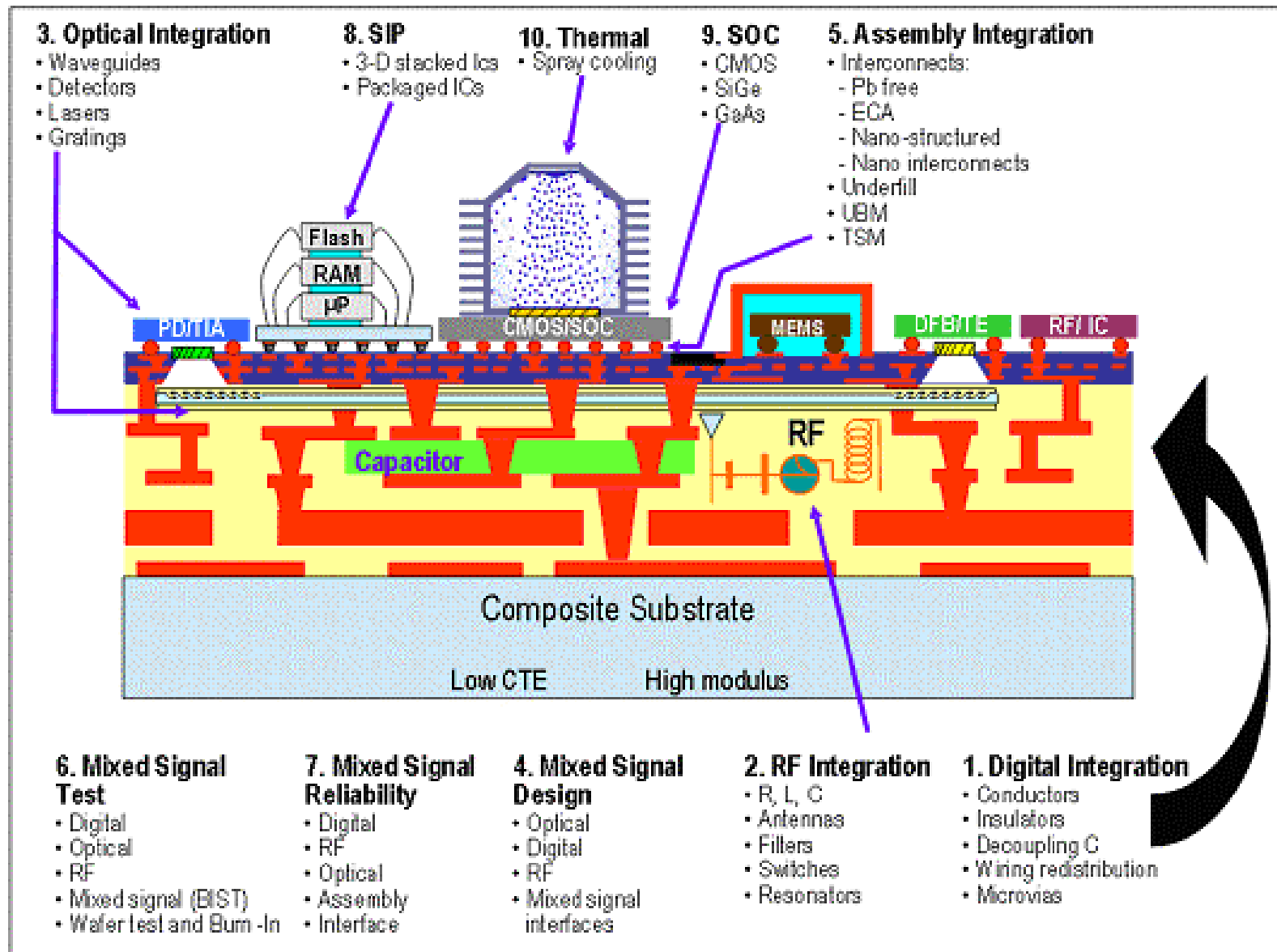


- **Market:** In 2004, 1.89 Billion SiPs were assembled. By 2008, this number is expected to reach 3.25 Billion, growing at an average rate of about 12% per year.
- **Technology:** SiP applications have become the technology driver for small components, packaging, assembly processes and for high density substrates.
- **Growth:** System in Package (SiP) has emerged as the fastest growing packaging technology segment although still representing a relatively small percentage of the unit volume.

- **System in Package (SiP) architectures have been developed and are now in full production.**
  - **Based on both organic and ceramic substrate materials**
- **This same architecture, allows for MEMS device construction with a variety of new applications.**
  - **Capability for buried cavities and channels**
  - **Fuel Cells and Life Sciences (DNA/Blood testing)**



Source: Professor Dr. Reichl, Fraunhofer IZM, Berlin Germany



Source: Professor Rao Tummala, Georgia Institute of Technology-Packaging Research Center.

<i>System In Package Requirements</i>												
<i>Year of Production</i>	<i>2004</i>	<i>2005</i>	<i>2006</i>	<i>2007</i>	<i>2008</i>	<i>2009</i>	<i>2010</i>	<i>2012</i>	<i>2013</i>	<i>2015</i>	<i>2016</i>	<i>2018</i>
<i>Digital networks- max I/O</i>	2600	2900	3000	3200	3500	3500	3500	3500	3500	3500	3500	3500
<i>RF products - max I/O</i>	150	200	200	200	200	200	200	200	200	200	200	200
<i>Max number of stack die</i>	6	7	8	8	8	8	8	8	8	8	8	8
<i>Max number die in Module</i>	10	12	12	12	12	12	12	12	12	12	12	12
<i>Minimum Component size in.</i>	0201	0201	01005	01005	01005	01005	01005	01005	01005	01005	01005	01005
<i>Die Pad pitch - wirebond</i>	40	35	35	30	30	25	25	25	25	25	25	25
<i>Die pad pitch - flipchip</i>	150	130	130	120	110	100	90	90	80	80	70	70
<i>Embedded Passives in Laminate</i>	L	L	CL	CL	CL	CL	CL	CL	CL	CL	CL	CL
<i>Embedded Passives in Ceramic</i>	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C
<i>MSL Level</i>	2a	2	2	2	2	2	2	2	2	2	2	2
<i>Mx Reflow temp C</i>	260	260	260	260	260	260	260	260	260	260	260	260

- **Segmented supply chain is leading to non-optimized cost effective packaging solutions and delaying the introduction of technology.**
- **Present materials supplier base does not have adequate demand (at a high enough sales revenue) to drive many of the needed R & D materials developments.**
- **The mechanisms for cooperation between industries and among researchers working in all advanced technologies must be strengthened.**
- **Cooperation between OEMs, EMS Firms, and component suppliers is needed to focus on the right technology and to find a way to deploy it in a timely, cost effective manner.**

- **Rapid market growth & technology advancement in RF subsystems is constrained by the pace of Research and Development of new:**
  - **Designs**
  - **Design tools**
  - **Materials**
  - **Manufacturing processes**
- **Needed for semiconductors, SiPs, RF components, & RF MEMS.**
- **Government, consortium, and academia needs to focus funding to address these R&D needs.**
- **Improved design tools for emerging technologies like embedded passives and optoelectronic PWBs.**
- **Development of automated printing, dispensing, placement, and rework equipment capable of the finer pitch requirements for SiP package assembly at current process speeds.**

- **Development of Low cost, higher thermal conductivity, packaging materials such as adhesives, thermal pastes, and thermal spreaders.**
- **Development of new approaches to organic substrate fabrication which address needs for dramatic increases in density, reduced process variability, improved electrical performance, and radical reductions in cost.**
- **Establish an iNEMI SiP Technology Implementation Group (TIG) to develop a research and development plan for closing the SiP gaps identified in the roadmap.**



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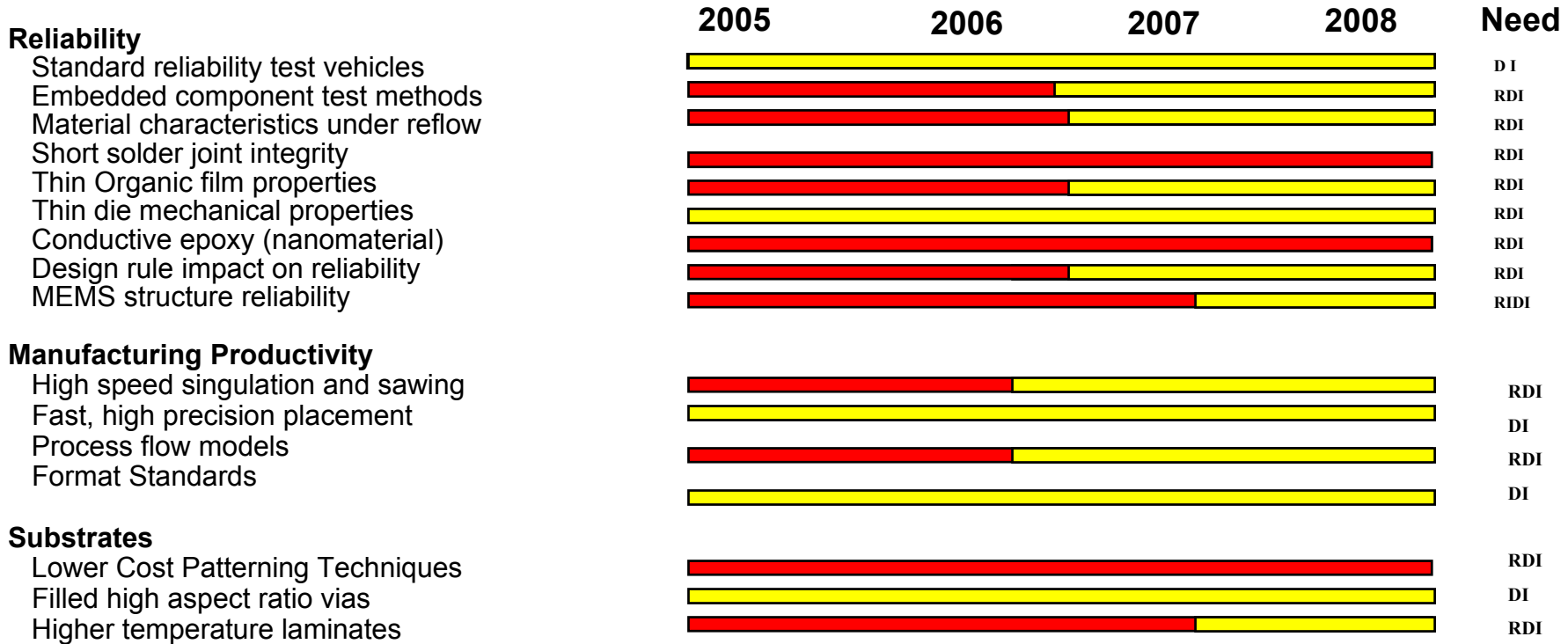
# System in Package Technical Plan



**Chair: Joe Adam, Skyworks**

- **Developed focus areas for Gap Analysis:**
  - **Reliability**
  - **Substrates**
  - **Materials**
  - **Equipment**
  - **Design Tools**
  - **Standards**
- **Completed a Technical Plan with Prioritized Gaps**
- **Next Step:**
  - **Organize Projects to Close the Gaps**

- **To identify research projects which have the highest impact on SIP development, are executable, and will get broad support**
  - There are many gaps which may not be addressable through the iNEMI project structure
  - The list of possible projects is very long with lots of competing approaches so finding common project interest is a critical objective
- **Identify sponsor companies within iNEMI and target companies for recruitment into iNEMI research projects**
  - Most of the leading SIP companies are not iNEMI members



X = Not Req'd  
 R = Research  
 D = Development  
 I = Implementation

█ Technology Sufficient     
 █ Technology—More Dev. needed     
 █ Critical Need for R&D

- **System In Package Reliability Projects**
  - **Thermal mechanical modeling of complex SIP structures and materials combinations**
  - **Development of passive component test methods for embedded components in mold compounds**
  - **Analysis of materials properties under reflow conditions**
  - **Lead free solder joint integrity in embedded SIP applications**
  - **Solder joint reliability for low stand-off solder joints in**
  - **Very thin organic film materials properties and adhesion mechanisms in this epoxy bonds**
  - **Thin die mechanical properties under varying surface conditions**
  - **Analysis of electroless finish plating solder joints**
  - **Interfacial resistance of conductive epoxy pastes**

- **SIP Manufacturing Productivity Improvement Projects**
  - **Alternative singulation techniques**
  - **Mechanical sawing process development**
  - **Alternative die attach techniques – electrically & thermally conductive films**
  - **Factory Standards**
  - **PCB solder mask to mold compound adhesion measurement methods, correlation to CSAM**
  
- **SIP Substrate and Interconnect Technology Projects**
  - **Low cost patterning techniques for interconnect**
  - **Drilling processes**
  - **High frequency design and simulation tools for RF and mix signal design**
  - **Low cost mixing of high frequency with high power dissipation**

- **Problem – There are no common test vehicles across industry to enable correlation new material, design rule, process, device, and applications R&D projects**
- **Proposal – Develop a set of standard test structures which are made available to industry for R&D evaluations**
- **Key Tasks**
  - **Define design rules set for each major technology element**
  - **Define a range of materials and processes types to be used**
  - **Identify key test methods and reliability evaluation objectives**
  - **Define sources for design, materials, and processes who can to support test vehicle design and fabrications**
  - **Build and distribute first generation test vehicles to project teams for test method development and testing**
  - **Set-up topic teams for review of each set of test data**
  - **Recycle through process to develop new vehicles based on results**

- **Key Challenges**
  - **Will companies be willing to openly share data on “failures”**
  - **Is there enough common knowledge on the problems that a group can agree on what the potential high priority areas of research are and resource these projects**
  - **SIP technology capability is a competitive advantage today for many companies so will they be willing to give up some of they advantage to get R&D leverage**
  - **Attract Volume drivers to become members of iNEMI (Agilent, Amkor, ASE, Foxconn, Fairchild, Epcos, Infineon, Murata, Phillips, RFMD Raytheon, Renesis, ST, STATSchippac, Skyworks, TDK, Triquint)**
  - **SIP is a very broad technology bucket with lots of small market niches so the market opportunity for materials, EDA, equipment and other infrastructure companies is small today**

- **iNEMI has demonstrated the ability to address supply chain/technology gaps in many other areas.**
- **We have identified some large gaps in SiP technologies which companies have a common interest in pursuing.**
- **Many of the research topics are complex and application specific so we will need experience applications expertise to drive activities.**
- **Decisions on which projects should proceed need to be made:**
  - **Need to attract the critical mass of companies to address gaps**
  - **Participation from members and recruiting will drive this decision over the next months**

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