



International Electronics Manufacturing Initiative

**Board Assembly  
Technology Working  
Group (TWG) Roadmap**



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*Productronica*

- **Board assembly incurs most of the direct-material costs for electronics products and is critical to electronics supply chain**
- **Identified areas for improvement:**
  - **Efficiency and utilization of high mix/low volume lines**
  - **Set up times & adoption of factory information integration with real time optimization**
  - **Ramps to volume and line flexibility**
  - **Qualification processes for materials & process development**
  - **DPMO leverage to understand package performance**
  - **DFx tools integrated with factory data systems**
- **Board assembly is being impacted by MEMS, optoelectronics and wireless communications packaging technology development**
- **Movement of board assembly to low cost areas of the world – primarily China – continues.**

Parameter	Definition	2003	2005	2007	2009	2015
Digital Terminals	Maximum number of terminals to the board. That are carrying a digital signal per package	800	2900	3200	3500	3500
RF Terminals	Maximum number of terminals to the board. That are carrying a RF signal per package	100	200	200	200	200
Maximum Body Size	(L x W)- mm	40	52.5	70	70	70
Minimum Terminal Pitch BGA	Pitch of the I/O (mm)	1.27	0.80	0.80	0.65	0.50
Minimum Terminal Pitch CSP	Pitch of the I/O (mm)	0.65	0.50	0.40	0.40	0.30
Number of stack die	Maximum number of stacked die in a package	4	7	8	8	8
Number of die in SiP max	Maximum number of stacked or unstacked die in a package	8	10	12	12	12
		0201	0201			
Embedded Passives	N/A	Few	YES	YES	YES	YES
MSL Level	Moisture sensitivity level per IPC that packages are qualified	3	2	2	2	2
Max Reflow Temperature	Common reflow temperature for multi die packages. – deg C	250	260	260	260	260
Die Attach Materials	Thermal conductivity critical	80%	85%	90%	90%	90%
	Low temperature capability	<5%	<5%	<5%	<5%	<5%
	Pre-applied	<1%	3%	5%	20%	30%
	Matched CTE capability	0%	5%	7%	15%	25%

### Key

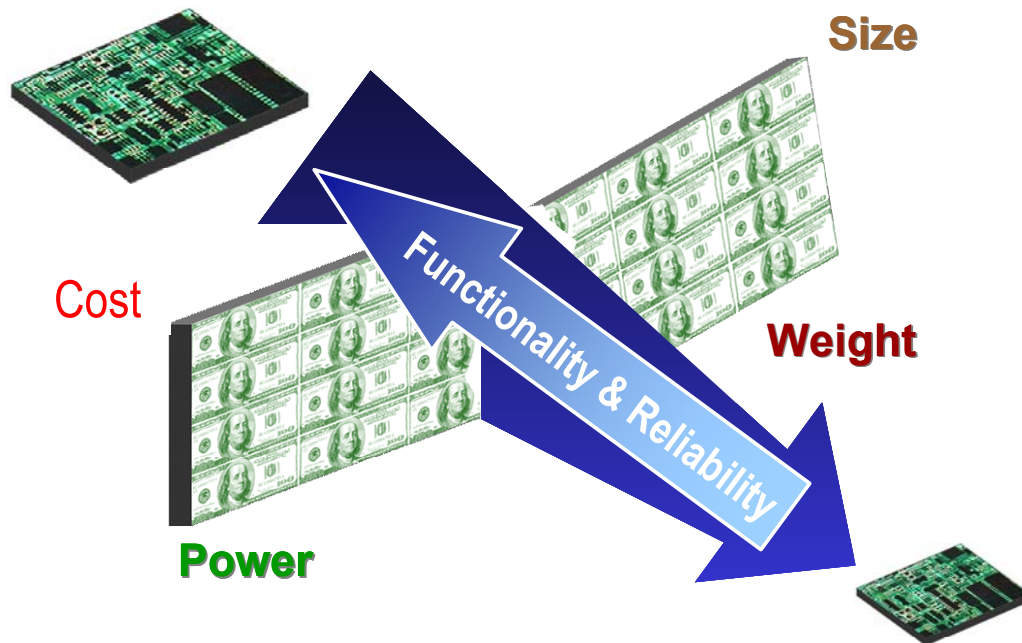
Current Capability

In Development

Research Needed

## Evolutionary Gaps

- **Manufacturing Challenges from Miniaturization**
- **Materials Reliability**



- **Improved stencil technology or paste dispensing**
- **Cost effective under fill process including rework**
- **Equipment to close cost gap between flip chip & SMT placement**
- **SMT compatible optical assembly processes with accuracies  $< 10 \mu\text{m}$**
- **Test procedures for optical components & electro/optical systems**
- **Analog test including scan and self-test technology.**

## **iNEMI Technical Projects**

- **Establish a SiP TIG to address process, materials, equipment, & reliability gaps.**

## **Design**

- **Develop improved design tools for emerging technologies like embedded passives and optoelectronic PWBs.**

## **Manufacturing Technology**

- **Develop automated printing, dispensing, placement, and rework equipment capable of the pitch requirements for SiP package assembly at current process speeds.**

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