Impact of Low Temperature Solder on Electronic Package Dynamic Warpage Behavior and Requirement

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***Abstract*—Low temperature solder (LTS) adoption has increased over the years with the primary focus on reducing energy consumption. The fundamentals of dynamic warpage are well established in SMT industry, but there is minimal literature on the application of low temperature solders, specifically for SAC BGA with low temperature solder paste. iNEMI has conducted a wide range of dynamic warpage characterization of different electronic package types, namely package on package, fine pitch BGA, large FCBGA package with and without lids, and a wide selection of PBGA packages. The database generated has been reviewed to understand the impact of low temperature solder on dynamic warpage considerations which avoids the typical maximum peak and valley warpage present at higher reflow temperatures. Additional consideration should be given to the rate and magnitude of contour change during LTS solidification phase that can induce a solder hot tear defect. It was found that mostly the PBGA and FCBGA package require greater attention and optimization for LTS adoption.**

Keywords-component; warpage, low temperature solder, FCBGA, PBGA, POP, FBGA

I. INTRODUCTION

Electronic packaging has been evolving rapidly during the last decades to enable new devices and new market segments. , Many of this made possible by component suppliers developing electronic packages that meet stringent requirements. Electronic package warpage needs to be managed to ensure the final product can be easily assembled on the board by original device manufacturers (ODMs). The drive to greener and lower energy consuming SMT processes has motivated the industry to assess the impact of low temperature solder on electronic devices.

Since the adoption of lead-free Tin-Silver-Copper (SAC) solder more than a decade ago, managing electronic package dynamic warpage has been a major focus area. Process conditions include higher reflow temperatures and lower ductility of SAC compared to leaded solder systems in SMT. Some electronic package constructs which demonstrate a higher sensitivity to temperature change such as Plastic Ball Grid Array (PBGA) packages can suffer yield detracting SMT defects like solder bridging and non-contact opens. Advances in the areas of alloyed solder material has led to the introduction of low temperature solders (LTS) which melt and solidify at a range of temperature from 130°C to 200°C, creating a new opportunity to lower the reflow temperature which inherently reduce the energy demand and may favor the dynamic interaction between package warpage and solder phase formation.

An iNEMI Project focusing on Bismuth-Tin (BiSn) based LTS Process and Reliability (LTSPR) was formed in 2015 to address the challenges of various LTS pastes covering a multiple alloys and chemical formulations manufactured by suppliers. The projects had three phases [1]. The LTS process considered was SAC BGA attached on the package with LTS paste screen printed on the board for SMT. Phase I entailed the selection of applicable pastes and a determination of the SMT processing ability of twelve formulation of LTS pastes in three metallurgy categories were selected for characterization. These metallurgies include (i) three types BiSn based eutectic pastes with 0%, 0.4%, and 1.0%wt Ag, (ii) five non-eutectic ductile BiSn pastes and (iii) four kinds of Joint Reinforced Pastes (JRP) resin containing BiSn eutectic solder compositions pastes. The JRP provide polymeric reinforcement of cured resin at the base of the formed joints; whereas the chemical formulation of the first two categories were very important for paste wetting and joint forming performance [2]. Subsequently, these thirteen pastes, which include the SAC as reference, been applied into the SMT processing parameters defined to focus on the characteristics of the mixed SAC–BiSn solder joints formed. High density BGAs, QFN and Sockets with SAC BGA were assembled to PCBs using BiSn solder pastes at peak reflow temperatures significantly below the liquidus temperatures of SAC solder balls. The challenges of LTS adoption and SMT parameters optimization opportunity were discussed and proposed in [3] based on the experimental results. One of the key defects highlighted in adopting BiSn based LTS paste is the hot tearing defect of mixed SAC-BiSn alloy solders which was observed in FCBGA joints located at the die shadow area when using four of the twelve LTS BiSn pastes. Hot tearing is thought to be caused by an interaction of Bi stratification at the package interface coupled with dynamic warpage of the FCBGA package as it cools from peak reflow temperatures. It

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can also occurred without Bi stratification if the solidification temperature overlaid with the package substrate package warpage shape inversion temperature [3]. Hot tearing defect is a critical concern and solutions may exist to enable LTS in SMT process as an attempt to mitigate yield and reliability associate to high dynamic warpage behavior. Extension to this assembly study of LTS, Phase III evaluated the predefined mechanical shock test of Package on Package (PoP) with SAC BGA coupled with BiSn based and JRP based paste joints. The study shows that BiSn and JRP based were weaker than homogeneous SAC BGA on the mechanical shock test condition highlighted in [4]. With extensive evaluation of LTS metallurgy system, there is a need to better understand and quantify package warpage behavior, This paper leverages many types of electronic package's dynamic warpage characteristics and the results from the LTSPR project to understand the implication of LTS to the electronic package dynamic warpage behavior and requirements.

II. PLETHORA OF DYNAMIC WARPAGE DATABASE

TABLE I. PACKAGE TECHNOLOGY CONSIDERED

Package Type	*Design*	*Schematic drawing of package construction*
PoP	Overmold Through Mold Via (OM TMV)	
	Expose Die Mold TMV (EDM TMV)	
	Bare Die PoP	
	Interposer PoP	
	Pre-stack PoP package	
	MCeP®	
	PoP Memories	
SiP	Overmold Multiple Chip Package (MCP)	
FBGA	Overmold single die package	
FCBGA	with single or multi dies	
FCBGA with Lid	Organic and ceramic substrate	
PBGA	Ranges	

Since iNEMI has conducted a wide range of dynamic warpage characterization of different electronic package types as shown in TABLE I. , namely the Package on Package (PoP), System in Package (SIP), fine pitch BGA (FBGA), large FCBGA package with and without lids and a wide selection of PBGA packages, the data collected [5]-[7] is further analyzed to establish the impact of LTS on dynamic warpage requirement. The dynamic warpage data was collected as discussed in [8]. The high temperature warpage requirement for SAC system has been well understood and some been tabulated in design guides, JEDEC with the failure mode associated to SAC system typically limited to solder bridging, non-contact open and head on pillow (HoP). The requirement of dynamic warpage proposed for low temperature solder is not only governed by the maximum peak and valley warpage values at peak reflow temperature but the rate and magnitude of change during solidification phase of low temperature solder also needs to be evaluated, as highlighted in [3]. This shows that SMT defect for LTS system can relate in a different way to dynamic warpage of the package.

III. IMPACT OF SAC SOLDER AND LOWTEMPERATURE SOLDER ON DYNAMIC WARPAGE

A. *Reflow Profile and Critical Temperature Points*

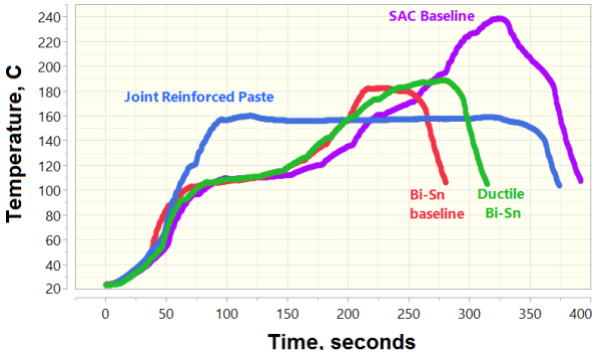


Figure 1. Typical reflow soldering profiles for SAC baseline, BiSn baseline, Ductile BiSn and Joint reinforced (resin) pastes.[2]

Most BGA packages come with SAC based solder ball attached and the implementation of LTS is mainly focusing on the use of BiSn based solder paste for PCB assembly. The typical reflow profiles depicted in Figure 1. overlays the SAC baseline reflow profile with the other three LTS paste types employed during the iNEMI LTSPR studies. The SAC baseline, eutectic BiSn baseline, ductile BiSn, and JRP were studied to provide fundamental understanding of the solder joints formations. Typical SAC based SMT reflow targets three key thermal ramp ranges of temperature, namely (i) Initial ramp, (ii) Soak approaching reflow, (iii) Rapid Ramp to melting and peak temperature, and (iv) Final Cool ramp down. Initial ramp is intended to bring the PCBA as a whole up to sufficient temperature to activate the flux chemistry so as to clean and prepare the solder pad surfaces for wetting. The slower soak time is timed to allow sufficient duration for the flux to react but not so long as to fully consume it and expose the solder pad surfaces to oxidation before wetting of liquidus solder. The soak also brings the entire PCBA thermal mass to near reflow temperature without significant temperature deltas across. The rapid ramp typically starts within 10°C to 20°C of solder melting temperature, 217°C for SAC305 and continues to peak reflow temperature which is

typically around 245°C to 260°C. The Time above Liquidus (TAL) is critical to ensure all solder volumes reach liquidus and all chemistry volatiles and voids can escape from the molten solder. Too short of a TAL can create HoP and non-contact open defects along with excessive voiding. Too long can damage the PCB and/or components and promote excessive IMC growth which in turn can increase the brittleness of the formed joints. The rapid cool down is targeted at improving grain structures, increasing throughput, and minimizing IMC generation at the joint interfaces of PCB and package pads. The LTS, namely as BiSn and Ductile BiSn, is mimicking the SAC baseline reflow profile but with lower peak temperature of approximately 182°C while the LTS solidification temperature ranges from 150°C to 125°C. The JRP reflow profile is uniquely different from the rest as the long soak requires to condition the resin and molten solder differently. However, the JRP paste used in [2] was not promising. Hence, JRP is not a key focus in this discussion.

B. Dynamic Warpage Interaction with SMT Defects

Electronic package dynamic warpage behavior has been the key assessment for this study. The typical warpage behavior that changes with temperature is shown in Figure 2. In this graph, there are three general dynamic warpage characteristics for Package A, B and C. Package A dynamic warpage is best resembling a typical PBGA package while the Package B and C resemble a typical FCBGA package. Package A started off as a concave shape (-ve) and transitions to convex as the temperature increases. Package B and C started off convex shape (+ve) and transition to concave shape. The difference between Package B and C is mainly the magnitude of warpage at higher temperature where Package C has higher peak temperature warpage.

Based on the earlier discussion on the SAC and LTS reflow profile, the dynamic warpage requirements or metrics may be different from LTS system. Firstly is the reduction of peak reflow warpage from 260°C to ~182°C; secondly the reduction of warpage at a point of initiation of solder solidification of LTS at ~150°C as compared to eutectic solidification of SAC solder at ~220°C; third is the warpage change during the LTS solidification phase between 150°C to 125°C where the solder may be deformed as it cools and lastly is the warpage change slope and shape inversion from convex to concave or vice versa. These temperature points were considered because of the availability of existing data of dynamic warpage for various packages. Each of these metrics is mainly for quantification of impact of LTS on dynamic warpage requirement and perhaps explain the benefits and considerations of adopting LTS paste based on the dynamic warpage response of the package. Apart from dynamic warpage behavior, the package rigidity at LTS solidification phase temperature is expected to be higher compared to SAC solidification temperature due to the increased structural stiffness of the package at lower temperature which exert greater tensile and shear stresses on the solder joints. This could potentially lead to hot tearing defects mentioned earlier. Although the PCB board warpage is also part of the equation and also needs to be evaluated, it is out of the scope of this paper. The following sections demonstrate the impact of LTS on warpage metrics mentioned which is an extension of the prior dynamic warpage collected in earlier phases of iNEMI project listed here [5]-[7].

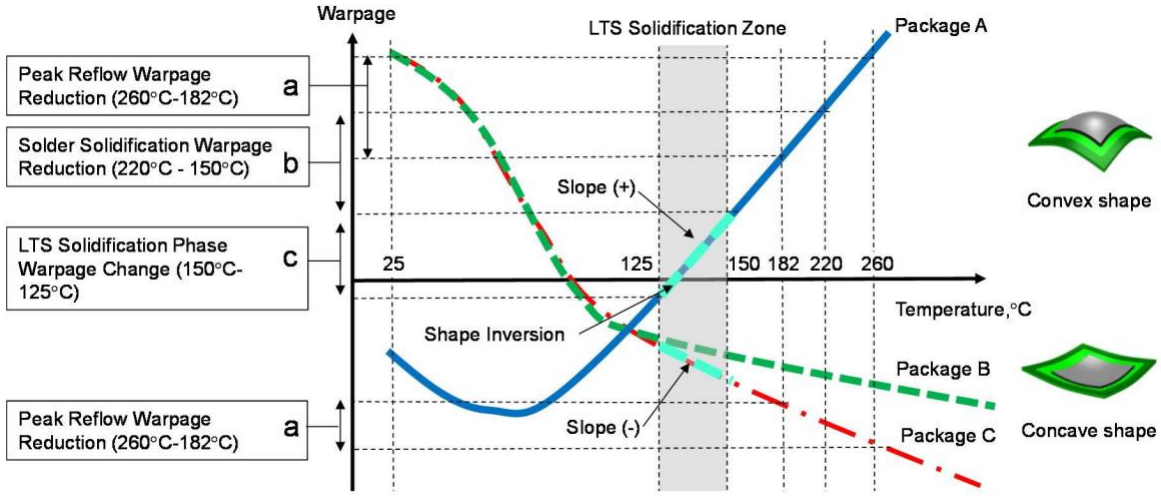


Figure 2. Typical Dynamic Warpage Behavior and LTS key characteristic

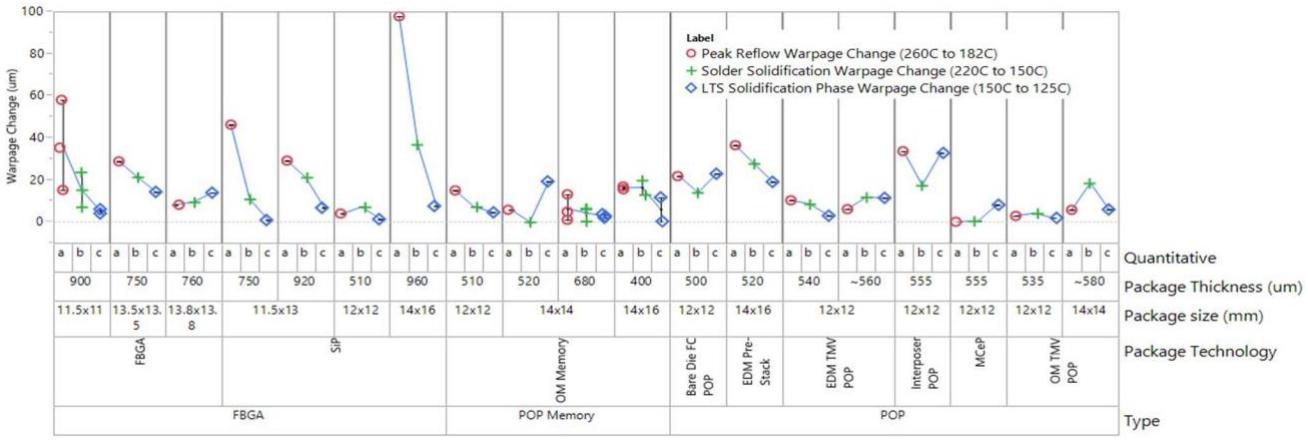


Figure 3. Package on Package and FBGA families warpage magnitude change

IV. Results and Discussion

By leveraging the past collected dynamic warpage data across various package technologies, each of the warpage changes as a result of reduced peak reflow temperature, solidification temperature and solidification phase of LTS were processed. This processed data provides an overview of the changes in warpage from a SAC solder system to a LTS system. In the following sections, each of the package technology families is presented by comparing the magnitude changes. There are other factors like design, materials used and package construction which can result in very different dynamic warpage characteristics and it's behavior using LTS. This is not included in this study Package on Package and FBGA families

The dynamic warpage of various types of Package on Package (PoP), PoP memories and FBGA are categorized together due to it small package size of less than 20x20mm. The raw dynamic warpage data can be referred to [5][6]. The original data was collected at different temperature readout and some was provided by participating companies which was processed with best fit interpolation for specific temperature readout required to compute the warpage changes discussed. 0shows the magnitude based on the three quantification methods. Each data point here represents an average value for a given type of package technology with similar package attributes. For FBGA package, the peak reflow warpage change (O marker) ranges from ~100um to ~5um; while for solidification warpage change (+ marker) ranges from ~25um to ~5um and lastly the LTS solidification warpage change (◊marker) ranges up to 20um. This suggest that a LTS system can have a impact to the warpage change and the adoption of LTS has minimal impact to the SMT yield quality because of minimal overall change of warpage magnitudes.

As for PoP memory, the warpage quantification of change for these is minimal with less than a 20um change. Since PoP memory was designed or optimized to pair up with a bottom package, the warpage of the PoP memory can have a bi-modal distribution of shapes (concave and convex) hence the average magnitude change is kept to a minimum. The adoption of LTS on PoP memory attach is still not widely practiced and hence the assessment here may not be relevant. For PoP package, the peak and solidification warpage magnitude change range within 40um. There are a few type of PoP packages namely the MCeP and OM-TMV that demonstrated less than 10um warpage changes suggesting that the LTS reflow has little effect on package dynamic warpage behavior. This can be explained due to the unique balancing of package design and material selection used to keep the dynamic warpage minimal for better adoption to PoP memories as well. For Interposer PoP packages, the solidification phase warpage change is relatively higher compared to the rest which may suggest the increased potential for hot tearing during the solidification phase of LTS.

A. *FCBGA families*

FCBGA package technology consists of two distinct categories namely the single die version represented as FCBGA and multi-chip package which is represented as FCBGA MCP as shown in Figure 4. For FCBGA, the package size ranges from 20x20mm up to 37.5x27.5mm while the package thickness ranges from 800um up to 3.7mm. The peak and solidification warpage change for package size of less than 29x29mm is less than 30um. For package size greater than 29x29mm, the warpage change is up to 60um. As for the LTS solidification phase warpage change, the FCBGA package shows up to 60um change as well which is similar to the change of peak reflow and solidification warpage change. This may indicate the higher risk of hot tearing which requires further validation. In general, the thinner and larger package exhibited higher warpage magnitude change.

For FCBGA MCP, the peak reflow warpage change is higher which ranges from ~90um to ~135um. This is higher than the single die version mentioned earlier because the larger and thinner package geometry. The data shows about 60um warpage change at solidification temperature. The LTS solidification phase warpage change is about 40 to 60um for the 40x24mm package size. This warpage change may post some challenges to manage the deflection of the substrate while stretching the solder joint to induce the hot tearing defect, especially when fine BGA pitch is adopted.

B. *FCBGA with Lids families*

The FCBGA package with Lids database is shown in Figure 5. which consists of organic and ceramic substrates. The change peak reflow warpage for these type of packages seems minimal despite the large package size ranging up to 55x55mm coupled with package thickness from 1.13mm to 4mm. The peak reflow warpage change of up to 50um and the warpage during the solder solidification is below 25um. The change of warpage during the LTS solidification phase also kept below 20um. Unlike packages without Lids, the warpage changes

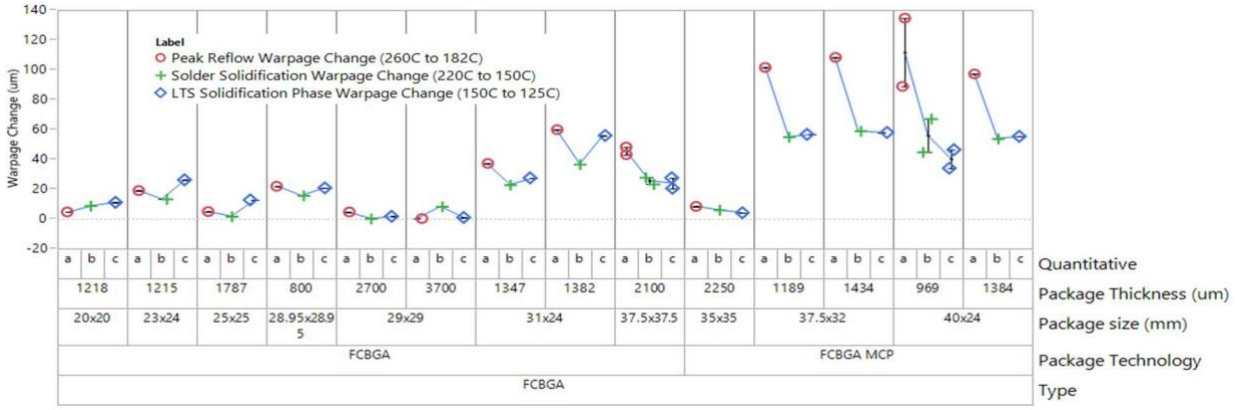
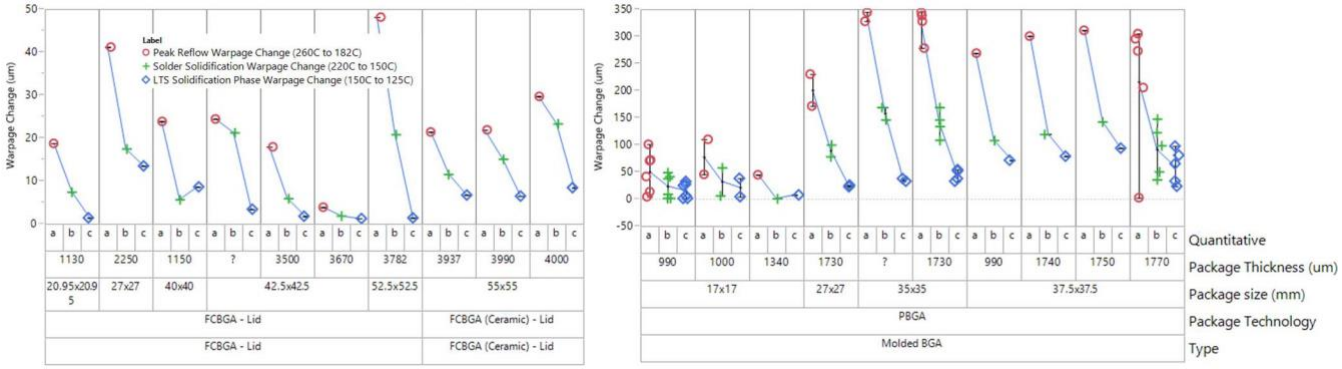


Figure 4. FCBGA families warpage magnitude change.



(a) FCBGA with Lids (b) PBGA Package

Figure 5. FCBGA-Lids and PBGA Warpage Magnitude Change.

from SAC system to LTS system is minimal. With such large packages, the ball pitch and ball size used are typically larger and hence the magnitude change can be considered a fraction of solder ball height. This may suggest the LTS adoption in FCBGA with Lids may not have gained significant impact to warpage change nor will it result in higher SMT yield lost. The adoption of LTS for such package seem seamless but further validation may required.

C. *Plastic Molded Ball Grid Array (PBGA)*

PBGA package constructs consist of significant volume of mold as an encapsulation over the wire-bonded dies. The dynamic warpage of PBGA is unlike those typical of the FCBGA package where the warpage starts off either in convex or concave shape at room temperature and turns to convex shape at reflow temperature [6]. Figure 5. shows the quantification used to understand the considerations in adopting LTS. Firstly, the peak reflow warpage changes up to 350um for the larger package size of 35x35mm and above. For smaller PBGA packages of 17x17mm, the peak reflow warpage can be changed up to 120um. The solder solidification warpage change ranges up to 160um for package sizes greater than 27x27mm. For 17x17mm package size, the solder solidification warpage change is within 50um. The LTS solidification phase warpage change can range up to 100um especially for those larger package sizes. The change of peak reflow and solidification warpage is highest among the package technology considered here. This seems to support the challenges of large PBGA package technology in adopting to higher reflow temperature during the transition from PbSn to SAC reflow[9]. On the other hand, the warpage change during the LTS solidification phase may post some

challenge in managing the potential hot tearing phenomena which requires further validation and actual SMT assessment.

D. Overall Warpage Change due to LTS reflow profile

Due to the diverse type of electronic packaging technology considered here, comparing the magnitude change can be a challenge as each package has its unique dynamic warpage characteristic. Hence the percentage of warpage change in adopting to a LTS solder system with reference to the SAC peak warpage reflow at 260°C is considered here. Figure 6. shows the percentage of warpage change for these families of package technology. The markers denote the trending of the warpage change where not all types of packages experience a reduction of warpage as a result of adopting LTS. For PoP and FBGA packages, the warpage change ranges from negligible impact to a factor of ~1000%. This extreme change is due to the warpage at LTS is a few magnitude order higher than the warpage at 260°C[7]. This, however, reflects the change of warpage percentage and not the absolute warpage magnitude. Majority of the package warpage change is as low as 10% to about 100%. For FCBGA and FCBGA MCP packages, the majority of the packages considered show about 20% to 100% warpage reduction and a few show warpage increases as well. This reduction seems reasonable as the results of 30% to 50% warpage reduction was reported in [2]. As for FCBGA with lids, the percentage of warpage reduction is about 20% to 50%. The even lesser change for large packages is mainly due to the constraint from the lids coupled with thicker constructions. Lastly for PBGA packages, the majority of them shows a warpage reduction from 40% to 250%. This higher warpage reduction seen in PBGA is attributed to the higher sensitivity of the package to temperature as a result of the higher volume of mold encapsulations used.

E. LTS Solidfication Phase Warpage Slope and Shape Inversion

In earlier sections, the warpage reduction and change were presented to provide an overview of the impact of LTS. Two other parameters that can be considered are the LTS solidification phase warpage slope and the shape inversion during the cooling down from 150°C to 125°C. Figure 7. shows the magnitude of the slope for each of the package technology presented earlier. The slope can range from ~-2um/°C to ~+4um/°C. The shape inversion describes the change of shape from convex to concave or vice versa. The magnitude shows the aggressiveness of warpage change with temperature during the solidification phase of LTS. At this range of temperature which is below or around the glass transition temperature of the substrate or mold, the stiffness of the package is higher which result in greater reaction force being exerted on the LTS joints. The result of this stresses can promote hot tearing defects. Based on the graph, the PBGA package with larger package size followed by FCBGA MCP packages exhibits increased risk of experiencing solder hot tearing due to higher slope and in some cases coupled with shape inversion. The + and - signage used on the slope axis will determine the region of hot tearing. For positive slope, the warpage change is towards concave. Hence the hot tearing region may appear at corner joints of the package. On the other hand, the hot tearing may appear in region below the package center or underneath the die shadow region because warpage shape change is toward convexity. The shape inversion can elevate the risk level of hot tearing which was presented in [2] where FCBGA package have seen such hot tearing underneath the die shadow at which cooling of the solder joints are relatively slower compared to peripheral joints. Also the shadow of the silicon die or dies also defines a line of sudden change in stiffness. Region beyond the die shadow is expected to allow for freer relative movement which may reduce the stresses on the joints. Hence, the adoption of LTS with range of solidification temperature requires further assessment to understand the mechanism and region of risk of hot tearing.

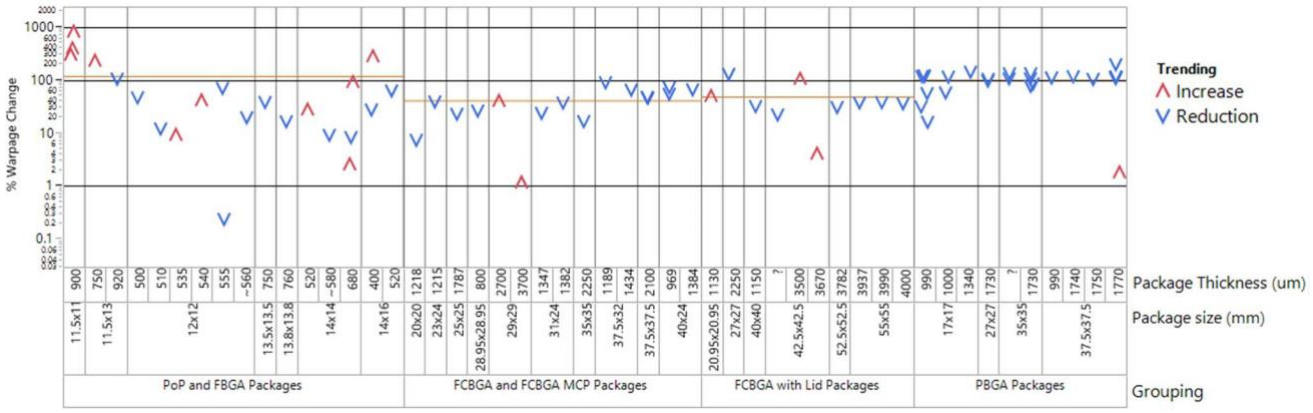


Figure 6. Overall peak reflow waragpe reduction percentage

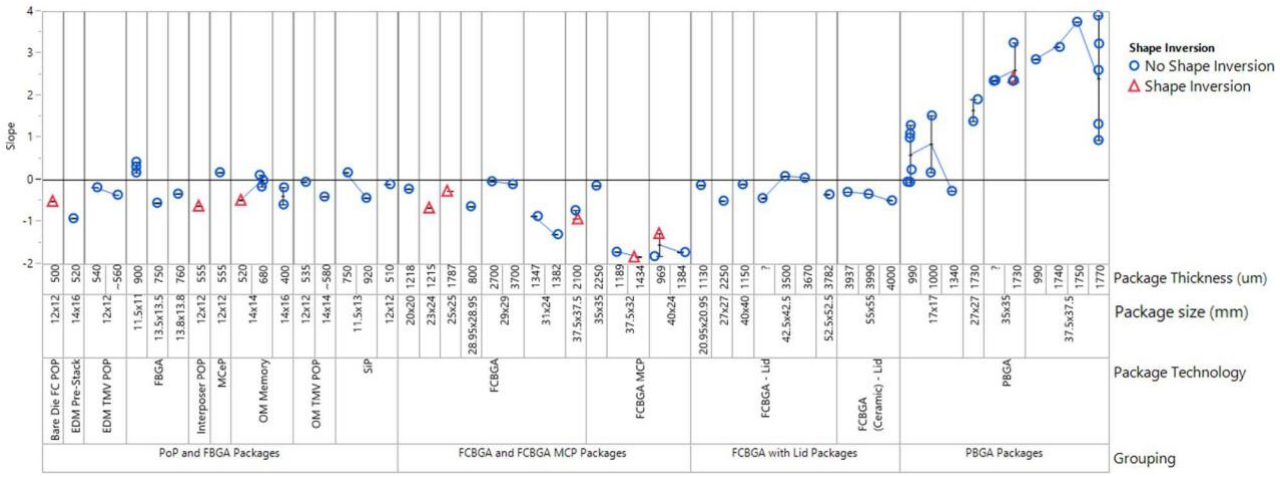


Figure 7. LTS Solidification Phase Warpage Slope at 150°C to 125°C and Shape Inversion

V. SUMMARY

Based on increasing adoption of LTS solder systems in products built, the consequences of dynamic warpage of electronic packages can be different from eutectic solder such as SAC systems. In most cases, the peak reflow warpage and solder solidification warpage reduces in magnitude, depending of package type and design construction. The LTS solidification phase happens in a range of temperature which concurrently coupled with the change of warpage magnitude and shape that elevate the risk of hot tearing. Such phenomena requires additional assessment in the industry. As part of providing an overview of the assessment, the warpage change during LTS solidification phase and the slope provide some indication of the risk of getting the hot tearing defect at either at package center or corner or edges. Based on the database gathered, the challenges to using LTS for PBGA packages need to be carefully considered. The percentage of warpage change for each of the package families provide an estimation of the impact of LTS and not all packages experience a reduction of warpage magnitude as a result of adopting LTS. The slope of warpage change and package shape inversion during LTS solidification phase can play a role in the potential of inducing hot tearing defects. The SMT risk assessment for these packages requires an effort from the SMT industry to characterize and understand the underlying risk of hot tearing and other SMT defects that encompass the effect of multiple reflow process and percentage of LTS paste to SAC solder volume. With initial work by iNEMI LTSPR project, there could be a solution in place to manage these defects through other means of optimizing SMT parameters as mentioned in [2].

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