

iNEMI New Package/ Material Qualification Methodology Project

End-of-Project Webinar / February 19, 2020

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Introduction

- During iNEMI's 2016 Substrate & Package Technology Workshop in Singapore, the following were identified as major gaps in the packaging industry
 - Lack of understanding of the device assembly processes and application environments of all potential end-users (vs targeted end-users) affects the development of effective reliability test methodologies for new package technologies and materials
 - Test plans only focus on standard test methodology and comply to customer requirements
 - Current test standards may not capture the reliability risk in the new package, or may over-stress the new package
 - Data about field failures are not captured in a way that provides feedback to the test plan
 - For new materials/package development, test plan completeness is always questionable
 - Little industry effort to develop new test standards

Introduction

- Past issues with standard qualification plans that were used for assessing new technology
 - Variability of bond pad structures and strength for qualification of Cu wire bonding
 - New failure mechanism and unique manufacturing controls for embedded IC packages
 - Are we sure that the standard test plan is able to detect and characterize all weak points in a new technology?

Introduction

- iNEMI officially started the industry project “Methodology for Qualifying New Packaging Technology” in July 2017 to address the gaps identified
- The purpose of this project is to develop a methodology for defining qualification plans for new packaging technology to address the gaps resulting from:
 - Lack of understanding of the assembly processes
 - Lack of understanding of the interactions of the materials and components within the new package
 - Lack of understanding of the application environment
 - Lack of understanding of the use conditions of all potential end-users
 - Lack of understanding about how variations of the manufacturing process could affect product quality and reliability

• Project timeline

- Review of current industry qualification standards - October 2017
- Completed the generation of the questions for the first survey - March 2018
- Conducted the first survey – March to June 2018
- Results and analysis of the first survey presented at IEMT2018 conference in September 2018 in Malaysia
- Conducted the follow-up survey – Dec 2018 to Jan. 2019
- Presented summary at ICEP2019 Conference in April 2019 in Japan
- Whitepaper & Final report – Feb 2020
- Present project findings and recommendations at IEMT2020 conference in September 2020 in Malaysia

Current Industry Standards Overview

- Shown below are several industry standards commonly used to qualify devices in new IC package technology and materials
 - qualification plans, tests methods, and pass/fail requirements

Standard Number	Standard Title
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
JESD94	Application Specific Qualification Using Knowledge Based Test Methodology
JEP150	Stress-Driven Qualification of & Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components
AEC Q100	Stress Test Qualification for Integrated Circuits
IEC-60749-43	Guidelines for IC reliability qualification plans
Mil-Std-883	Test Method Standard for Microcircuits
Mil-Std-750	Test Methods for Semiconductor Devices

- None of these industry standards address
 - The entire process for qualifying a new package technology/material
 - Which industry best practices should be used, e.g.,
 - How to identify best material set
 - Initiate Failure Mode and Effects Analysis (FMEA)
 - Assess all possible customer assembly and field conditions

Lesson Learned – Historic Issues with New Materials & Package Technologies

- Halogen-free mold compound – Red Phosphorus
 - Passed qualifications by many device suppliers and took one or more years before failures first started to occur
- Copper Bonding Wire
 - Propensity for bond pad cratering is a function of bond pad structure which can vary within a device, and thermosonic stitch bonds can fail if lead finger delamination expose them to humidity and contaminants
- Pb-free reflow temperatures and IMC formation
 - Switch to Pb-free solder balls on BGAs accelerated the growth of the IMC layer for some gold ball bonds on Al bond pads due to multiple high temperature excursions (reflow simulations) and certain substances in the composition of some mold compounds

Lesson Learned – Historic Issues with New Materials & Package Technologies

- Pb-free solders

- Solder pumping of flipchip bumps (secondary reflow) when there is delamination of or voids within the underfill
- Solder joint fracture occurred when consumer electronics were dropped, bulk of initial testing of Pb-free solders focus on fatigue life and not resistance to shock (drop testing).

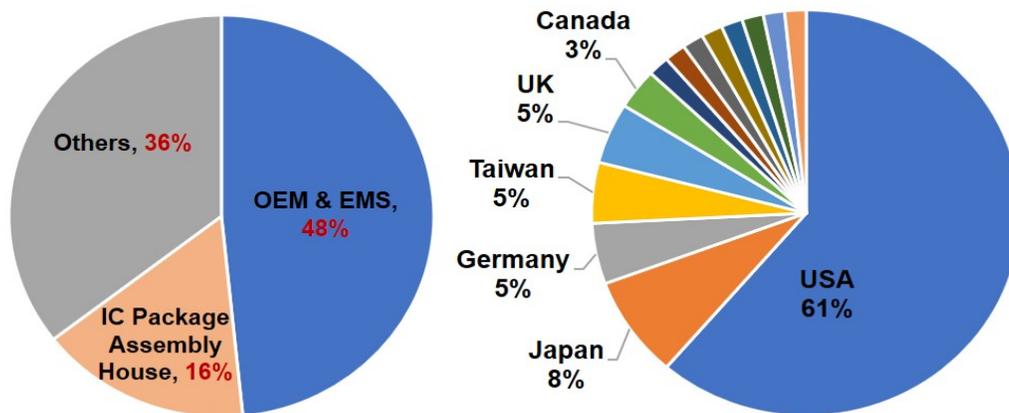
- ENIG (black pad)

- Surface finish for pads on BGA substrates were not tested robustly enough to assess the possible variability in electroless Ni immersion Au plating process controls, specifically phosphorus content.

Survey Scope and Respondents

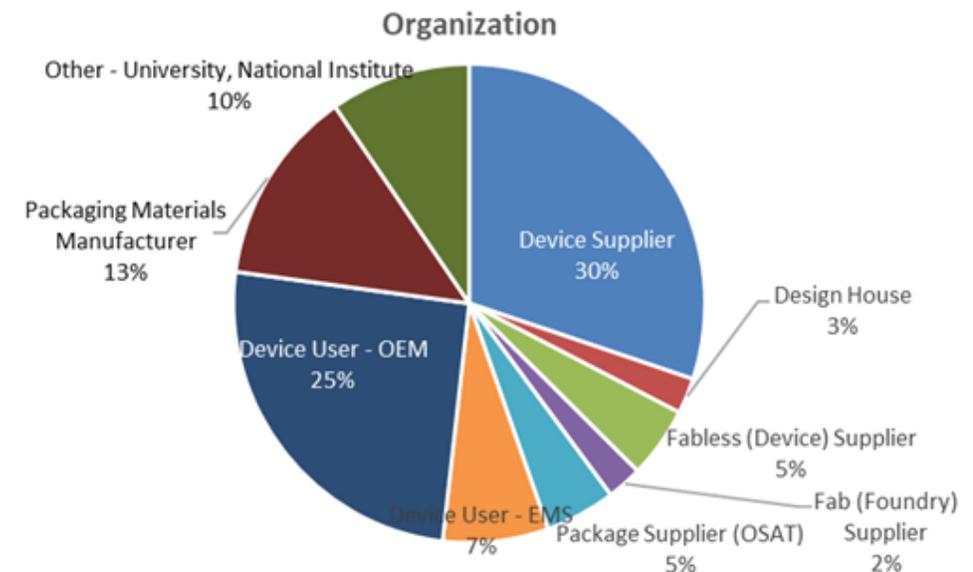
The First Survey

- The first survey consisted of 7 sections covering the qualification requirements and methodologies used to develop and qualify new package technologies and new materials
- A total of 62 responses were received for the first survey



The Follow-up Survey

- The follow-up survey attempted to obtain detailed information in a few key areas, specifically new package technologies and application spaces
- A total of 92 responses were received for the follow-up survey



Survey Summary

- The results of the two surveys highlighted that there is a discrepancy between supplier and customer knowledge on the use of new technologies and materials, the application conditions of where it is used, and the details of the qualification that was performed
 - This discrepancy highlights the need for greater sharing of information between companies, from technology and materials used within a device, to the range of application conditions, and finally to the details of the qualification process and its results.
 - The awareness of what failure mechanisms could occur with new package technology and how best to test for those mechanisms can be improved and would greatly benefit from the generation of an industry guideline of best practices.
 - This difference in understanding and use of qualification methods throughout the supplier chain confirms the need for an industry guideline of best practices.

Survey Summary

- The surveys highlighted differences between field use conditions and the qualification stress conditions required to support those use conditions.
 - Respondents highlighted that application use temperatures are rising, with some going higher than the current 150°C upper limits
 - A few going below the -65°C lower limits
 - The fact that survey respondents have extended their test durations indicates an awareness that improvements are needed to industry test methods and qualification standards
- Several new application spaces are also recommended, here are two:
 - Wearable electronics (skin contact, oils, flexibility)
 - Automotive – immersed in engine fluids (e.g., antifreeze, oil)
- Device users pointed out a large discrepancy in what information was provided in a qualification report
 - This highlights the need for better communication across all members of the supply chain from end users back to package development teams.

White Paper Background

- Over the years the qualification of new package technology and materials has shifted from OEMs, to device supplier, and now to package assembly OSATs
 - May now be 2 or 3 companies between the company developing new package technologies and materials and the company that designs and sells the system that will use it
- Majority of today's electronic devices, including those that incorporate new package technologies and materials were originally designed and qualified for consumer electronics
 - Once qualified and in use, new package technologies and materials are available for other devices regardless of their application space

White Paper Background

- Today, the standard device qualification report shows passing results that fulfill the requirements of industry qualification standards for consumer electronics applications
 - This is sufficient for manufacturers of consumer electronic products
- It rarely show the complete history and/or learning that went into the qualification of the new package technology and/or materials that was incorporated into a packaged device
 - They do not contain all of the insight regarding the techniques used, lessons learned, initial fails, and additional stress data
 - This additional information is what manufacturers of high reliability products require to ensure that the new package technology and/or material will meet the application requirements of their product

White Paper Background

- What is lacking is a document that addresses the qualification process itself for new package technology
 - Multiple qualification standards exist for various application spaces.
 - Many books and more papers exist that describe package technology as well as qualification techniques, tools, and best practices
 - JEP001, “Foundry Process Qualification Guidelines”, are three documents that form a qualification methodology for IC fab processes
- The methodology will be a repository for all of the best practices and provide background on why and when to use a specific stress or test, what to consider when developing a qualification plan, and many other aspects required for evaluating and assessing new package technology

Highlights of White Paper

- Contents of Methodology
 - Understanding and Identifying all Use Conditions
 - Tools and Best Practices
 - Assessment prior to reliability tests (Usability, not reliability)
 - Qualification Standards and Test Methods
 - Qualification Reports

Highlights of White Paper

- Understanding and Identifying all Use Conditions
 - Manufacturing (device assembly to board, board into system)
 - Varies greatly by product type and complexity
 - Soldering temperatures, flux, washing, bakes, cures, board flexure, shock & vibrate
 - Shipping (device, system)
 - temperature/humidity exposure, shock, and vibration
 - Field
 - wide range of simultaneous and sequential environmental and operating stresses, including long storage durations
 - Operational: Mechanical, thermal, and electrical current
 - Environmental: thermal extremes and cycling, moisture, chemical, vibration, mechanical shock, gravity/acceleration, and radiation

Highlights of White Paper

- Tools and Best Practices

- 3 Step Qualification Process

- Technology Assessment, Technology Qualification, Device Qualification

- Simulation (FEM – Finite Elemental Modeling)

- Assess reaction to thermal, mechanical, and/or electrical stress
- Aids in material and design evaluations

- FMEA (Failure Mode and Effect Analysis)

- Risk analysis tool for assessing both product design and manufacturing processes

- Test chips vs. Functional devices

- Specially designed test chips are more sensitive than “functional” die in detecting minute changes in “package induced” mechanical stress on the die as well as changes in electrical responses due to material fatigue or moisture/corrosion

Highlights of White Paper

- Tools and Best Practices

- Detailed construction analysis

- Can provide quick insight into potential quality and reliability issues and overall workmanship.
- Non-destructive x-ray and acoustic microscopy provide 1st pass analysis of samples identifying which should receive destructive analysis and where to focus analysis
- Inspection of decapsulated/opened packages (visual, SEM, and other tests)
 - Wire bonds, die attach, underfill, passivation integrity, bond pad cratering, etc.
- Inspection of cross-sections, including some after fluorescing dye penetration
 - Wirebond IMC formation, integrity of flipchip joints, wirebonds, die attach, IC, leadframe or substrate, encapsulation material, hermetic seal, etc.
 - Defects: voids, delamination, migration/corrosion, cracks, dicing, singulation, etc.
- Other tests: BGA ball shear, solderability, external visual, coplanarity/warpage, etc.

- Detailed and well “thought out” failure analysis

Highlights of White Paper

- Tools and Best Practices

- Electrical characteristics

- Assess trade-offs/constraints for package design and materials; and their affect on impedance, resistance, and inductance requirements for the target applications

- Test to failure

- Is only technique for identifying new failure mechanisms for new package technologies and materials
 - Only technique for generating acceleration models

- Sequential Stress Testing

- Assess combination and interaction of real-life humidity and thermal stresses

- Safe Launch

- Increased testing, sampling, and screening of initial production to ensure that no new failure mechanisms or yield detractors were missed during qualification

Highlights of White Paper

- Assessment prior to reliability tests (Usability, not reliability)
 - Moisture/reflow sensitivity (J-STD-020)
 - Assess how absorbed moisture affects a packaged device during reflow soldering
 - Potential issues include delamination, cracks, warpage
 - Defects may cause immediate, intermittent, or long term reliability fails
 - MSL Classification vs. Preconditioning (JESD22-A113)
 - Process flow and evaluation criteria in J-STD-020 is different from that in A113
 - Reflow profile for good solder joints vs. J-STD-020 evaluation profile
 - The reflow profile in J-STD-020 is a “typical”, worst case profile and should never be used as a model for actual PWB assembly
 - Profile development for PWB assembly should be based on optimal solder joint formation

Highlights of White Paper

- Assessment prior to reliability tests (Usability, not reliability)
 - Moisture sensitivity vs. Process Sensitivity (J-STD-075)
 - J-STD-075 accesses and classifies devices that cannot be exposed to the full thermal profile defined in J-STD-020
 - Duration of some parameters in the thermal profile in J-STD-020 is a range
 - J-STD-075 evaluates devices against the extremes of the J-STD-020 reflow profile
 - Process sensitivity
 - Uses 3-character code plus additional information to describe process limitations
 - Thermal limitations are more prevalent to some passive device types, but some IC devices may have process limitations for flux exposure, water washing/immersion, and x-rays just to name a few
 - Package warpage during reflow (JESD22-B112)
 - New, complex packages may warp in unexpected ways during reflow operations

Highlights of White Paper

- Qualification Standards and Test Methods
 - Qualification standards for packaged devices
 - JEDEC (IT and consumer electronics)
 - AEC (Automotive)
 - JEITA (Automotive and general)
 - IEC (Aerospace to consumer)
 - SAE (Aerospace, military, and high performance systems)
 - Test Methods
 - For reliability projections: Thermal Cycling/Shock, Biased Temperature and Humidity, High Temperature Storage, Power Cycling, Unbiased Temperature and Humidity (HAST and Autoclave), Electromigration of 1st level interconnect
 - Assessments: Shock and Vibration, Hermeticity, Salt Spray, Corrosive Gases

Highlights of White Paper

- Qualification Reports

- Requirements of a qualification report
 - Intent of a qualification report is to provide the customer with the necessary information to be able to determine the suitability of the package technology to be used in their application
- Why aren't JESD69 or AEC-Q100 formats more widely used?
 - Majority of customers manufacture consumer electronics, whose requirements are well understood by device suppliers and industry qualification standards
- How to interpret and use the information in a Qualification report
 - Qualification report may combine results for multiple materials, facilities, and devices for new package technology, but must provide detail to allow the customer to confirm whether all of the assumptions are appropriate for their application.
- Qualification by similarity

White Paper Summary and Recommendations

- The white paper is a “first draft” of a document that is hoped to be adopted by an industry standards body
 - The intent is that industry experts will make it a living document that is reviewed and updated on a regular basis.
 - The next step is to initially offer the draft to JEDEC to publish and maintain
 - But in no means does the project team intend to prevent any other industry organization from participating in its development and future growth.

Project Summary & Next Steps

- This project was initiated with concerns on
 - The tendency of moving the assessment of new package technology and materials from device suppliers to subcontracted packaging houses
 - Qualification plan would most likely only focus on the requirements of the initial customers but not on all potential application spaces
- The project team partook in three separate tasks to address these concerns
 - Document commonly used qualification standards used today and some of the more notable “Lesson Learned” in the IC packaging world that the aforementioned standards did not catch.
 - Generated and conducted two industry-wide surveys to get a broader understanding of needs and practices
 - Generated an initial draft of an industry white paper documenting a methodology for the development, assessment, and qualification of new package technology and materials used in IC devices.

Project Summary & Next Steps

- The project's team's recommendations to standard bodies that generate IC device qualification standards and test methods
 - Review these recommendations from the survey and assess whether your organization should take on the challenge of generating those documents which you feel you are best qualified
 - Reach out to other standards bodies to determine which organization is best qualified; or if deemed appropriate, work together to generate joint standards
 - Standard bodies have a more diverse membership (than our project team) and thus have better insight of the needs of their members and which have a higher priority
- The project has generated an initial draft of a methodology for assessing new package technology and materials and qualifying IC devices that incorporate them.
 - The project team's recommendation is that JEDEC completes the methodology and publishes it as a companion to JEP001, "Foundry Process Qualification Guidelines"

Project Summary & Next Steps

- The availability of detailed qualification reports is critical for OEM manufactures of products with high reliability requirements and with demanding application conditions
 - As several standards exist regarding the format and content of qualification reports, it is up to OEMs to reference these standards in contracts with their suppliers
- The old adage, "Those who cannot remember the past are condemned to repeat it.", aptly applies to IC packaging
 - Many test methods and qualification standards are developed to address past quality and reliability issues
 - The project team recommends that at a minimum that some form of the Lessons Learned be included with the Methodology.

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Document Availability

- A copy of this presentation should be available on the iNEMI website by the end of February
- A copy of the end of project report should be available on the iNEMI website by early March
- <https://community.inemi.org/content.asp?contentid=550>

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