Inspection / Metrology Evaluation of Fine Pitch Test Vehicles for Advanced Packages

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***Abstract*— The demand for integrated silicon packages is driving packaging advancements for increasingly fine circuit pattern designs. Due to the thinner copper and finer features required for advanced packaging, copper line defects can significantly impact yield and reliability. Industry Automated Optical Inspection (AOI) capabilities for packaging features are reaching detection limits.**

Phase One of the iNEMI metrology project surveyed industry capability and completed a gap analysis. This work established the basis for the current activities in Phase Two. A fine featured test vehicle was designed and fabricated using thin film processing technologies on both glass and silicon substrates to evaluate and assess the limits of today's AOI metrology equipment. The test vehicle also provided a platform to develop future metrology capability required to close the technical gaps with respect to product requirements and process and material capabilities.

The test vehicle samples were provided to various industrial AOI equipment suppliers to evaluate their capabilities in evaluating fine lines and spaces. The integrity of the fine wiring lines and spaces was compared between a control pattern and known defects utilizing wiring patterns from 10 µm lines and spaces to 1 µm lines and spaces. Various types of features including different orientations were evaluated: a) Line width violations; b) Spacing violations; c) Excess copper or missing copper; d) Shorts; e) Opens. This paper will review the details of the Phase Two test vehicle and the results from the AOI evaluations, and present a roadmap for the next phase of the study with test vehicles on organic substrates.

Keywords: Metrology, inspection capability, fine circuit pattern, defect detection

I. INTRODUCTION

Heterogeneous System-in-Package (HSiP) electronic packaging solutions are becoming more popular. These environments demand finer circuit pattern designs. However, optical inspection has limitations in feature size as well as in efficiency in detecting defects. This impacts the yield performance and quality validation on the laminate substrates and boards which are used for integrated SiP packages. Inadequate inspection capability of fine line and space geometries on panel sized substrates and boards which support high I/O high bandwidth memory and other fine pitch devices can seriously impact yield performance and reliability [1] [2].

iNEMI launched a collaborative project on Fine Pitch Circuit Design Inspection Metrology in 2016. The purpose of this project is to assess the measurement and inspection capability for fine circuit pattern substrates and boards used in high bandwidth applications.

Incorporation of fine pitch technology is new to the industry, and the iNEMI Phase 1 survey [3] highlighted how limited both manufacturing experience and capability are to most companies. There is significant interest to establish fine pitch design; however, the current inspection techniques are based upon wafer-level toolsets and the efficiency of the Automated Optical Inspection (AOI) tooling is not optimized for larger substrate packaging and printed circuit boards (PCBs). The AOI efficiency must be evaluated for substrate fine line and space designs in terms of defect rate capture and inspection. In addition, the AOI equipment must accommodate substrate packages in multiple form factors: singulated laminates that can range in overall size up to 150 mm or more in length, as well as strip format laminates with multiple substrates that are tested prior to separation based on final module assembly requirements. Depending upon manufacturing requirements, AOI must be developed to minimize the time for inspection while assessing required accuracy. Establishing the use of AOI for yield enhancement is the goal for manufacturing. Yield loss comes from defects that cause electrical failures (e.g. opens, shorts, resistance fails, etc.), from warpage and shape deformation that prevents further assembly or package function, from foreign material, and from spacing violations.

The introduction of a new technology requires comprehensive characterization. With fine line width and pitch wiring, there is both a measurement and an inspection requirement. There is a distinction between these two techniques. With measurement requirements, one must fully characterize the features and establish tolerances and norms. Inspection applies these measurement parameters to differentiate acceptable product from fails.

Measurement requirements include line width, line spacing, feature position, and warpage. The technology required to

measure fine pitch is evolving. Techniques such as optics, laser, and white light sources are being continually developed to handle increasingly fine dimensions. This survey indicated that the industry is also approaching wafer level measurement infrastructure for fine pitch circuit measurement and inspection. This requires a new generation of packaging measurement equipment.

The factors that determine the fine pitch design rules include device footprint and pitch, device I/O density, package cross-section and system design. iNEMI has a technology roadmap to drive organic substrate and board technology to achieve 2/2 (μm) & 1/1 (μm) line/space design rules. The anticipated benefits of the project are to provide guidelines of the inspection and metrology for the high bandwidth application substrate and PCB interconnects. This project includes two phases. In Phase 1, the project members conducted an industry-wide survey to assess the measurement and inspection capability and readiness for fine circuit pattern substrates. In the survey, fine pitch circuit patterns are defined as having features less than 15 μm and fine pitch micro bumps or conductive interconnect features with overall size below 15 μm in any dimension. The survey highlighted that there is a need for improved inspection for metrology and defect detection. The inspection capability on fine line (<=10μm) and space (<=10μm) features on panel size substrates and boards impacts both yield and performance capability. Fine line and space requirements provide high density interconnects (HDI) which support the high I/O bandwidth memory and other component integration for fine pitch devices. Defects include a) Line width violations; b) Spacing violations; c) Excess copper or missing copper; d) Short or open circuits; e) Interconnect pad integrity; and f) Line neck down. In addition, micro connect pad patterns were included to evaluate future development of small bumps. As a result of the survey, the team developed a design with fine featured lines and spaces to fabricate a test vehicle for AOI evaluation. The TV (test vehicle) design was fabricated in both glass and silicon substrates which were distributed to selected AOI companies to perform a study to benchmark current metrology and capability limitations.

II. Test Vehicle Design

Key features of the design include: line width, line spacing, line geometry, and defect detection. The range of 10 μm to 1 μm line width and spacing was chosen based on future high bandwidth applications. Since the current manufacturing capability is typically limited to 10 um line width and spacing in organic substrates, the test vehicle was constructed from semiconductor tooling using both glass and silicon materials in a wafer format, to achieve the targeted range for the AOI inspection. The test vehicle (TV) incorporated design features that simulated manufacturing defects which locally removed 20, 40, 60, 80% of the trace width (known as mouse bites) and simulated extraneous metal by adding protrusions which bridged 20, 40, 60, 80, 90, 100% of the gap between traces. The design implements arrays that include the following equal line widths and spacings: 10, 8, 6, 4, 3, 2, 1 μm. These same values were used as diameters of pads in the interconnect arrays. Table 1 lists the design features with an image showing an example of each feature.

TABLE I. Test Vehicle Design Features

Test Vehicle Features	
Requirement	**Image**
Sharp angle etch & dielectric	
Curvature	
Angled	
Rotation, Orientation	
Missing metal	
Extraneous metal	
Diameter	
Proximity to other features	

The test vehicle pattern was repeated across the wafer area to fully test the ability of the AOI equipment. Figure 1 provides the overall repeated pattern used across the wafer. Figure 2 highlights one cell of the various feature sizes. Figure 3 shows a full sample pattern repeated in a 12 x 23 matrix.

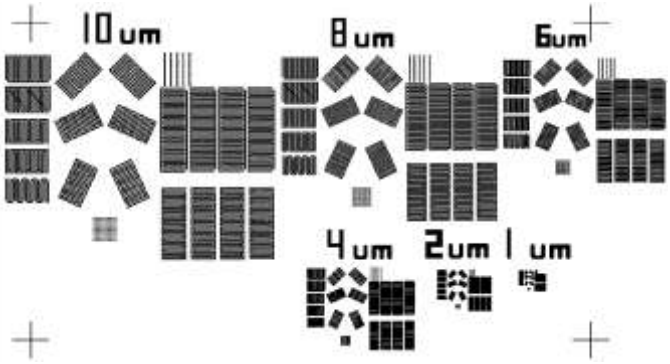


Fig. 1. iNEMI AOI TV Repeated Pattern

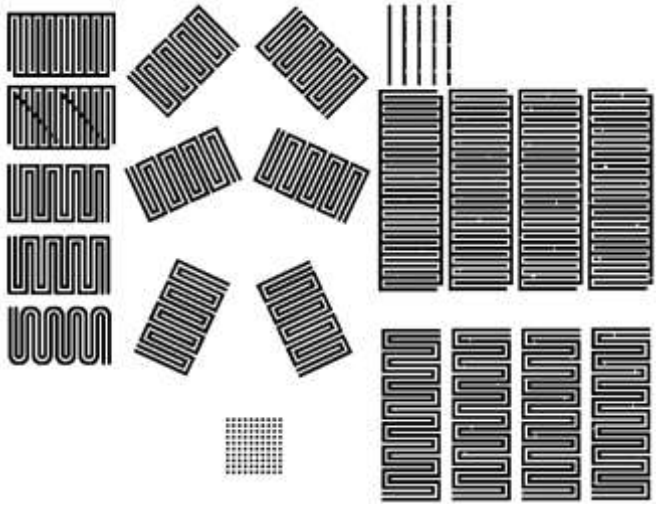


Fig. 2. iNEMI AOI TV One Cell Feature

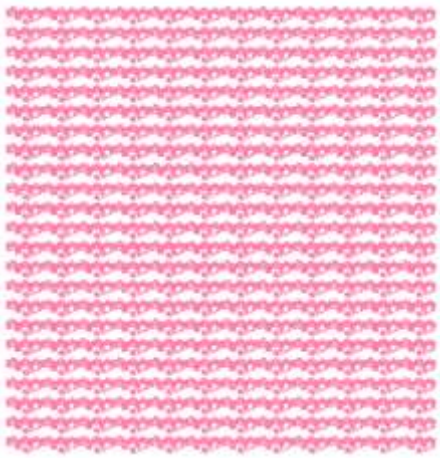


Fig. 3. iNEMI AOI TV Full Wafer or Panel Coupon Pattern

To validate the AOI detection of defects, a golden design was also created which removed the mouse bites and protrusions. The golden design could be used to inspect the trace quality.

III. Test Vehicle Fabrication

Technology for laminate fabrication at sub 10µm features is limited. First pass TVs used either a glass base or a silicon base material for ease of manufacturability and accuracy.

A. Glass TV Fabrication Process

For finer lines, it becomes necessary to select a smoother dielectric, such as glass. The challenge now becomes producing fine line metallization that adheres well on a smooth surface. The use of a sputter-deposited Cr/Cu seed layer that chemically bonds to the smooth glass surface provides optimum adhesion, especially for fine Lines/Spaces (L/S) circuit features produced during a Semi-Additive Plating (SAP) process. The process flow for a SAP process is shown in Figure 4(a). One can see the fine features produced in the photoresist layer prior to plating, as shown in Figure 4(b), and the resulting fine line Cu plated circuitry that this process produces, Figure 4(c). The use of SAP is capable of producing uniform sidewall Cu metal cross-sections for L/S below 10um.

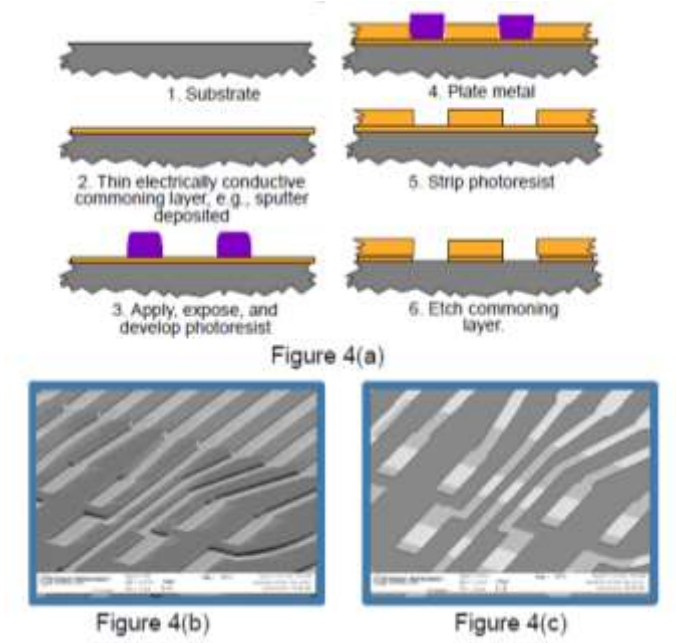


Fig. 4. Semi-Additive Plating Process for Glass TV

a) The major steps used in semi-additive plating. b) Shows the fine definition of the photoresist prior to plating. c) Shows the final Cu circuit lines after plating and removal of photoresist.

B. Silicon TV Fabrication Process

As a follow-up to the glass TV, a silicon wafer TV was created which provided similar optical opacity as an organic laminate. The silicon wafer was processed as shown in Figure 5.

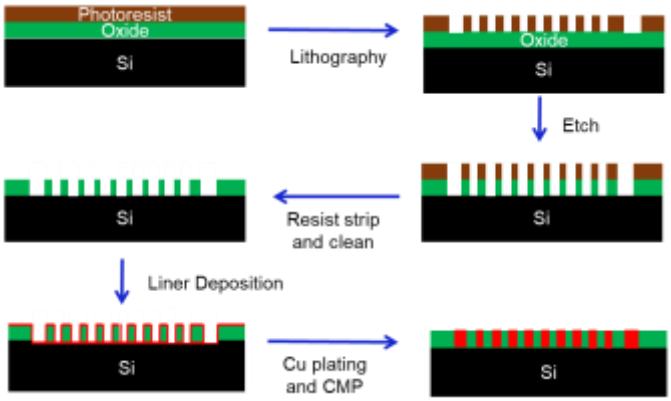


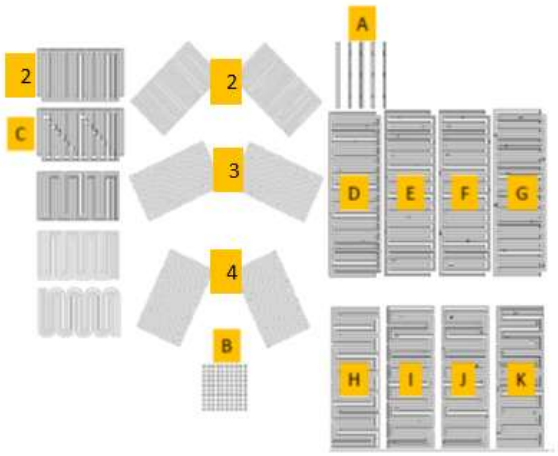
Fig. 5. iNEMI Wafer TV Process Flow

IV. Inspection and Reporting Procedure

Measurement guidelines and a reporting template were provided to the participating AOI companies so that the data could be collected and presented in a uniform format. The guidelines and instructions provided included the following:

- Measurement Items:
  - Line Width and Spacing
  - Defects in Features
  - Micro Bump
- Features evaluated:
  - Line Width and spacing:
    - TVs are designed with the patterns as follows: vertical, 60 degree angle (+ -), 45 degree angle (+ -), and 30 degree angles (+ -) => 7 locations
    - Two different traces in pattern
    - Total points in design: 7 features x 2 diff points = 14 measurement points in one design
    - Nominal widths in one Cell: 10 µm, 8 µm , 6 µm , 4 µm , 2 µm , 1 µm in total 6 nominals
    - 5 cells in a panel
    - Ground measurement points in a panel: 14 points x 6 nominals x 5 cells = 420
  - Defects in Features Inspection:
    - 2 Defects features are designed, which are mouse bites and protrusions.
    - Defects are designed in vertical traces and horizontal traces.
    - Golden design file is sent to all measurement sites.
    - The entire panel area including trace designs and defect feature zone is measured by AOI and compared with the AOI data and Golden design.
    - Report any abnormality in features after the comparison with photo and location (xy coordinate)
  - Micro Bump Shape Measurement:
    - Micro balls are manually placed at the inspection site.
    - Measure the shape and report the Diameter and Height with photo.

Figure 6 highlights the recommended defect pattern measurement locations.



Line Width Measurement Location:

- **1: Vertical Line:**
- **2: 45 degree line (positive & negative)**
- **3: 30 degree line (positive & negative)**
- **4: 60 degree line (positive & negative)**

Defects Measurement Location:

- **A: Mouse Bite (5 different degree) in vertical traces**
- **B: Micro Bump Shape**
- **C: Protrusion (5 different degree) in vertical traces**
- **D: 20% Mouse bite in horizontal traces**
- **E: 40% Mouse bite in horizontal traces**
- **F: 60% Mouse bite in horizontal traces**
- **G: 80% Mouse bite in horizontal traces**
- **H: 20% Protrusion in horizontal traces**
- **I: 40% Protrusion in horizontal traces**
- **J: 60% Protrusion in horizontal traces**
- **K: 80% Protrusion in horizontal traces**

Fig. 6. iNEMI Test Vehicle Defect Pattern Locations

V. RESULTS

The measurements from AOI companies were compared to Scanning Electron Microscopy (SEM) images taken of the design pattern. Figure 7 provides a representative SEM image of the 4 um features from the glass carrier sample. Table II provides the SEM baseline values for the two test vehicle structures.

A. SEM Measurement

The fabrication variations in trace widths and spacing were evaluated by SEM measurement, and these values are treated as the fabricated trace widths and spaces for the comparison with any AOI measurement data. The baseline values for the different sized features are also shown in Table II. The SEM measurements show that the feature widths are slightly oversized relative to their design point and the spaces are slightly undersized.

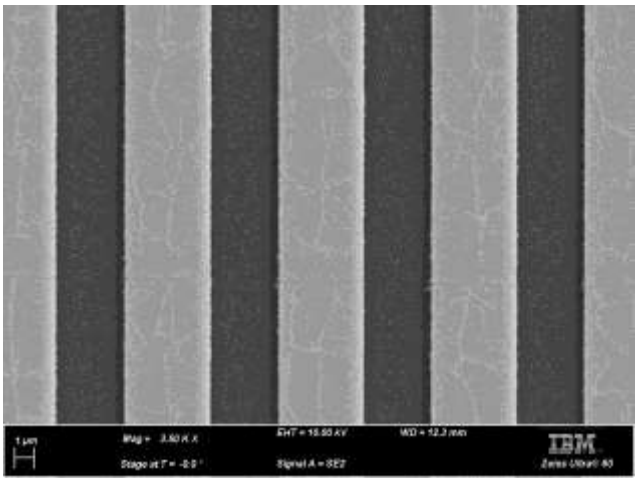


Fig. 7. SEM Image of 4um Test Vehicle Structure

TABLE II. TEST VEHICLE MEASUREMENT

SEM Test Vehicle Measurements				
Feature	**GLASS**		**SILICON**	
	Line	**Space**	**Line**	**Space**
1 um	Not Resolved		1.3	0.8
2 um	1.9	2.1	2.3	1.8
4 um	4.5	3.5	4.3	3.8
6 um	6.3	5.6	6.4	5.8
8 um	8.2	7.8	8.4	7.9
10 um	10.5	9.5	10.4	9.8

B. AOI Measurement

Six AOI companies and OEM labs participated in the evaluation of the equipment capability in line/space measurement and defect detection, covering both lab inspection and measurement equipment and production level inspection equipment. Final data from two of the six evaluations were received and is presented in this paper. The other four evaluation activities are still in progress at the time this paper was published. The final results will be included in a future publication.

1) Data Set A: Lab Tooling

Data set A was collected by an optical CMM (Coordinate Measurement Machine) that uses contrast / pixilation to capture line edges. The optical CMM is used for engineering analysis, and only has the capability of line/space measurement. Defect detection capability is not evaluated. Readings were taken at the locations specified in Figure 6. Resolution of the CMM is 1.5um as dictated by the stage, but within the field of view, it is better.

The measurement on the glass TV shows good accuracy with respect to SEM measurement data, as the edge measurement with back lighting enhances the accuracy. Greater deviation of measurement data on the silicon TV is observed, as back lighting technique cannot be used on silicon.

TABLE III. DATA SET A: GLASS TV MEASUREMENT

Glass TV (9 wafers, 240 locations each)			
	Lines-10	**Lines-08**	**Lines-06**
	um	**um**	**um**
Average:	10.57	8.56	6.53
Max:	11.79	9.94	7.56
Min:	8.86	6.50	4.92
Std Dev:	0.56	0.55	0.49

TABLE IV. DATA SET A: SILICON TV MEASUREMENT

Silicon TV (5 wafers, 240 locations each)			
	Lines-10	**Lines-08**	**Lines-06**
	um	**um**	**um**
Average:	8.67	6.27	4.72
Max:	12.60	9.54	8.82
Min:	6.88	4.78	3.13
Std Dev:	0.91	0.84	1.05

2) Data Set B: Production Tooling

Data set B was collected on leading-edge production level inspection equipment, which has capability of measurement and defect detection specially designed for PCB inspection.

One glass TV and one silicon TV were used for the evaluation. The equipment had excellent image acquisition on both samples and was able to detect all planted defects on 10, 8 and 6 microns lines (images of the defect detection are not included in this paper due to confidentiality agreement with the AOI company). Four (4) micron and smaller is beyond the capability of the equipment.

TABLE V. DATA SET B: SILICON TV MEASUREMENT

Silicon TV (1 wafers, 70 locations)			
	Lines-10	**Lines-08**	**Lines-06**
	um	**um**	**um**
Average:	9.94	7.80	5.81
Max:	10.48	8.36	6.32
Min:	9.38	7.44	4.96
Std Dev:	0.24	0.17	0.25

Line/space measurement was also performed on the silicon TV (shown in Table V). Similar to defect detection, the equipment was capable to perform measurements down to 6 micron lines with accuracy.

VI. CONCLUSION

The iNEMI Phase 2 Test Vehicle was developed to examine AOI readiness for fine pitch technology associated with high

bandwidth applications. Tighter integration, reduced real estate, system integration, and increased power delivery are factors challenging the industry with fine pitch circuitry. The main driving force towards fine pitch is increasing I/O and functionality. Fine pitch introduction will become a key enabler for high performance applications. Based on the iNEMI industry survey performed during Phase 1, participants indicate that fine feature inspection and measurement must be available within the next 3-5 years. This driving force also supports the ever-increasing device complexity. Secondary effects include reduced laminate dimensions, incorporating heterogeneous integration by accommodating multiple die/component interconnects, reduced substrate footprint, and minimizing substrate build up layers.

Incorporating measurement into manufacturing requires tooling that can comprehensively analyze characteristics of the wiring. To verify if a potential defect is acceptable, full analysis of the defect is required and follow-up reliability testing performed to assure that application conditions are met. Examining defects requires traceability to isolate failure modes and manufacturing problems. Traceability should be incorporated to identify individual part history, including lot number, date code, machine reference, and batch material constituents.

The available AOI data shows a reasonable comparison to the feature sizes established by the SEM analysis. The wide variability of the AOI data suggests that improvements are required in feature edge detection. The work highlights that AOI can be utilized for high volume manufacturing measurements and inspection for fine feature lines in various configurations. However, to date, features under 6um could not be effectively resolved by AOI. Since heterogenous integration (HI) is driving finer line and space geometry, developing AOI capability under 6 microns will be a key development action that the industry must meet.

VII. NEXT STEP

The planned Phase 3 of this project is a continuation from this Phase 2. The purpose of Phase 3 is to further characterize and quantify industry capability by conducting an inspection capability study and analysis using an organic substrate TV with fine line space features and defect patterns. The same ground rule for fine features used in Phase 2will be repeated in Phase 3.

Design and fabrication will be executed in panel form for Phase 3 to simulate the HDI substrate for HSiP. Inspecting organic materials is the challenge the industry faces, so this test vehicle will comprehensively examine AOI capability for practical use under the warped organic TVs.

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