Panel Session: Packaging challenges & opportunities for 5G applications

• Moderator: Dr. Haley Fu, iNEMI
• Time: 4:30-6:30pm, December 4, 2019
• Venue: Marina Bay Sands Singapore
Speaker Introduction

Prof. Yue Ping Zhang
Professor, School of Electrical and Electronic Engineering
Nanyang Technological University, Singapore
Antenna-in-Package (AiP) Technology for mmWave 5G Phased Array Chips

Y. P. ZHANG, FIEEE

Nanyang Technological University
Singapore
- AiP development driven by the need for novel antenna solution to RFIC

- CMOS for RF
  - JSSC 1986

- CMOS RFIC
  - ISSCC 1997

- Integrated circuit package antenna for RFIC
  - 1998

- First AiP Award to
  - Zhang, et al. at University of Cambridge
  - 2007

- AiP coined and published by Zhang
  - 2006

- First phased array AiP marketed by Sibeam
  - 2008

- First AiP invited paper by Zhang and Liu published in IEEE TAP
  - 2009

- Zhang, et al. awarded the Sergei A. Schelkunoff Prize for AiP by IEEE APS
  - 2012

- Historical note on AiP
  - IEEE AP Magazine Overview of AiP
  - PIEEE 2019

- Qualcomm AiP for mmWave 5G user equipment at ISSCC
  - 2018

- IBM AiP for mmWave 5G base station at ISSCC
  - 2017
Under intensive research recently by IEEE EPS
Having advanced to industrial reality (Incomplete list)
Creating a new industry sector and a market hot sport
AiP technology is the key to the success of mmWave 5G
- Smart™ AiP technology for mmWave 5G
- AiP technology will continue to be essential even beyond 5G

The evolution of mobile terminal antenna design
Key references for AiP technology

Editors
D. Liu and Y. P. Zhang
Antenna-in-Package Technology and Applications
IEEE-Wiley
March 2020

- AiP technology Wechat groups

The Antenna Academy
The Antenna Institute
The Antenna School

eypzhang@ntu.edu.sg
Speaker Introduction

Shunichi Kikuchi
Corporate Vice President
Fujitsu Advanced Technologies Limited
Panel Session: Packaging challenges & opportunities for 5G applications

December 4, 2019
Shunichi Kikuchi
Fujitsu Advanced Technologies Limited
DX that Fujitsu is pursuing

Digital data is bridging between consulting/services and technology/integration.
Values can be delivered to customers by disrupting the limitation of time and space.

- Secure and user-friendly finance service
- Modernized system
- Manufacturing innovation
- Enrichment of health and life
- Personized experience
- Safe and secure mobility society

Data

Consulting & Services

Technology & Integration

Base Station

5G

Computing

Cyber Security

AI

Cloud

HPC

Smart phone

IoT

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Material for 5G/IoT and other mm-waves

Higher data rate communication can be achieved with better antenna performance

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Warpage</th>
<th>Cost</th>
<th>Stack-up</th>
<th>Antenna performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.6GHz</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4.5GHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>26GHz</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>28GHz</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>39GHz</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>60GHz</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>77GHz</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>79GHz</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

Various material candidates for AiP

- LTCC (Low-Temperature Co-fired Ceramic)
- LCP (Liquid Crystal Polymer)
- PTFE (Poly Tetra FluoroEthylene)
- Ceramic-filled PTFE
- Glass-reinforced PTFE
- Glass substrate
- Organic substrate
- INFO RDL
- INFO WLP

Proposal from HPC design: measurement of Dk and Df

A balanced-type circular disk resonator

Specimen: □39.5±0.5mm(4-C3), 2 pieces
typ. 0.1-0.3mm in thickness

PWB organic material, glass, LCP, PTFE, ceramics, etc.

Measurement range: 10 - 95GHz, -55 - +150°C

Obtained Wave Form

Dielectric Constant (Dk)

Precise Analysis

Dissipation Factor (Df)
Proposal 2: measurement of Cu surface conductivity

Network Analyzer

A dielectric resonator method

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Anticipated benefit

Precisely measured properties are very useful to achieve the targeted goal. This approach can be applied to other products like 5G/IoT packages.

**Measured Dk/Df**

Catalog: Dk=3.643

Catalog: Df=0.004

**Measured Cu σr**

Copper pattern
200μm wide
30μm thick
20cm long

**Validation (Siml vs. Msmt)**

Simulated loss using catalog Dk, Df and σ

Using measured Dk and Df only

Using measured σ only

Simulated loss using measured Dk, Df and σ

Measured loss

---

Surface conductivity

Catalog: σ=100% of pure Cu

Interface conductivity

Catalog: σ=100% of pure Cu
Proposal: Measurement of EM strength in near field

Noise sources can be detected and shielding effect can also be confirmed.

An experiment of a tablet PCBA

- Measured magnetic strength
- Reproduced simulation result
- Simulated magnetic strength

DUT candidates

- Shield
- Compound Silicon

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Speaker
Introduction

Dr. Toshihisa Nonaka
Technical Director of Packaging Solution Center
Hitachi Chemical Co., Ltd.
5G related activity of Hitachi Chemical

Dec. 4, 2019

Toshihisa Nonaka, PhD.

Packaging Solution Center
Hitachi Chemical Co., Ltd.
Function of Packaging Solution Center (PSC) of HC
PSC Capabilities for 5G / RF Front end

Test vehicle designing

PCB-based module
- Flip-Chip Bonding
- Molding (Compression / Transfer)
- RDL fabrication

FO-based module

Material
- Low Dk/Df material - AS-400, LW-900 series
- Low Dk-Df substrate - HE-679G, HS-100 series
- Molding Compound - CEL(Granule), EB (Film)
- Underfill material - CEL(CUF), AZ (NCF), MUF
- Fine patterning RDL - AH/AR series

EM-field simulation

Antenna simulation

Transmission line simulation

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### Low Dk/Df Material Roadmap of Hitachi Chemical

#### Table: HCC Low Dk/Df material roadmap (Dk/Df @ 10GHz)

<table>
<thead>
<tr>
<th>Items</th>
<th>2019</th>
<th>2020</th>
<th>2021</th>
<th>2023</th>
<th>2025</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wire less comm. Gen</td>
<td>4G LTE</td>
<td>5G phase 1 (&lt;6GHz)</td>
<td>5G phase 2 (28-30GHz)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EMC/MUF</td>
<td>3.5/0.005</td>
<td>3.3/0.004</td>
<td>3.0/0.004</td>
<td>3.0/0.003</td>
<td></td>
</tr>
<tr>
<td>Embedding film(EBIS)</td>
<td>3.4/0.0032</td>
<td>3.2/0.0028</td>
<td>3.0/0.0020</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Substrate(Multilayer)</td>
<td>3.3/0.0028</td>
<td></td>
<td>3.0/0.0018</td>
<td>&lt;3.0/&lt;0.001</td>
<td></td>
</tr>
<tr>
<td>Substrate(Low CTE)</td>
<td>3.5/0.0035</td>
<td></td>
<td>3.1/0.0030</td>
<td>2.9/0.0025</td>
<td></td>
</tr>
<tr>
<td>Metal clad film(MCF)</td>
<td>3.0/0.0023</td>
<td>2.7/0.0019</td>
<td></td>
<td>2.5/0.0015</td>
<td></td>
</tr>
<tr>
<td>Photosensitive(Liq.)</td>
<td>2.8/0.0025</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Photosensitive(Film)</td>
<td>3.2/0.022</td>
<td>3.0/0.009</td>
<td></td>
<td>2.8/0.005</td>
<td></td>
</tr>
<tr>
<td>Expandable adhesive sheet</td>
<td>2.5/0.005</td>
<td>2.3/0.0024</td>
<td></td>
<td>2.1/0.0008</td>
<td></td>
</tr>
</tbody>
</table>
Substrate Core Material line up of Hitachi Chemical

Low Df

Low CTE

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Thermal Conductive Material Line up of Hitachi Chemical

- **HTR series** / Insulation adhesive paste (Thickness: 50μm – 2mm)
- **EN series** / High thermally conductive sheet
- **TC series** / High thermally conductive sheet
- **New Cu Paste** / High thermally Sintering Cu paste
- **HS series** / Thermally conductive DAF (Thickness: 20 – 30μm)
- **CEL series (EMC, MUF)**
- **EBIS series** / Insulation adhesive film (Thickness: 100 – 250μm)

**Insulation type**

- 180W/mK
- 40-90W/mK
- 10-20W/mK (20W/mK; Under development)
- 4-5W/mK (Under development)
- 3W/mK
- 3-8W/mK (>5W/mK; Under development)
- 1.5-2W/mK (Under development)

Thermally conductive level
Thank you very much for your kind attention!
Speaker Introduction

Erkko Helminen
Sr. Manager, Advanced Development - Corporate Technology
TTM Technologies
PCB Design and Fabrication Trends – Telecom, Networking & Computing

PCB designs heading towards convergence of RF & digital with a need for thermal management solutions

**Shrinking geometries**
- Imaging accuracy
- Plating quality
- Etching accuracy
- Lamination tolerance
- Drilling tolerance
- Registration & dimensional tolerances
- New process innovations
- Cu surface & oxide treatments
- Measurements

**Lower noise budget**
- Faster data rates
- Wide frequency range
- Hybrid stack ups
- HDI & Anylayer technologies
- Fine pitch for <0.5mm
- PCB with cavities
- High aspect ratio (1:20 – 1:25)
- Stub length ≤6±4mil
- Sub 3.5/3.5mil line/space
- Impedance Zo control ±5%
- Large format BGA (>70mmx70mm)
- PAM-4 requires tight Z control (RL)

**Complexity**
- Cu surface roughness
- Extreme low loss (FR-4) materials (Df<0.002)
- Spread and low Dk glass
- PTFE, LCP etc.
- Flexible materials
- Material properties and tolerances (e.g. Dk, Df, thickness, TCDk etc.)
- Skew (e.g. spread glass)
- Halogen free materials
- Dimensional stability

**Tightening tolerances**
- Inlay and different coin structures
- High thermal conductivity materials
- Heavy plated vias
- Via farms
- Flexes/rigid flexes
- Hybrid constructions
- New process & cooling innovations

**Lower total loss budget**
PCB Design and Fabrication Trends – Smart Phone and Portable Devices

Key smart phone PCB miniaturization drivers are; Increasing complexity of the advanced semiconductor package technology, battery capacity expansion & antenna integration and placement.

### Portable PCB/SLP Technology Trends

<table>
<thead>
<tr>
<th>Complexity</th>
<th>Integration</th>
</tr>
</thead>
<tbody>
<tr>
<td>4+N+1</td>
<td>mSAP/SAP SLIP</td>
</tr>
<tr>
<td>3+N+1</td>
<td>mSAP/SAP SLIP</td>
</tr>
<tr>
<td>2+N+1</td>
<td>mSAP/SAP SLIP</td>
</tr>
<tr>
<td>1+N+1</td>
<td>mSAP/SAP SLIP</td>
</tr>
</tbody>
</table>

- **Coaxial/Any Layer via**: Pad 75µm Via 100µm
- **Molded/Any Layer via**: Pad 200µm Via 100µm
- **1+1**: Pad 500µm Via 125µm

### HDI/SLP – Laser Drilling

<table>
<thead>
<tr>
<th>Diameter (µm)</th>
<th>Today</th>
<th>Development</th>
<th>Future solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>70</td>
<td></td>
<td></td>
<td></td>
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<td>60</td>
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<td>25</td>
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<tr>
<td>15</td>
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</tr>
</tbody>
</table>

#### Glass reinforced dielectrics
- Picosecond lasers (Ultra small via)
- Femtosecond lasers (Ultra small via)
- USP technology enables smaller HAZ

#### Non-reinforced dielectrics
- Nanosecond UV + CO2 process (Low via density/low volume)
- Nanosecond UV lasers (Low via density/Flex & rigid flex)

### HDI/SLP Pattern Formation & Imaging

<table>
<thead>
<tr>
<th>Imaging</th>
<th>SLP</th>
<th>HDI PCB</th>
</tr>
</thead>
<tbody>
<tr>
<td>DI &amp; LDI Exposure</td>
<td>Ultra thin dry film technology</td>
<td>Stepper exposure</td>
</tr>
<tr>
<td>Subtractive</td>
<td>Advanced subtractive</td>
<td>Advanced mSAP</td>
</tr>
<tr>
<td>mSAP</td>
<td>SAP (primer)/SAP (ABF)/SAP (Dry)</td>
<td>Embedded trace, coreless, etc.</td>
</tr>
</tbody>
</table>

### Key smart phone PCB miniaturization drivers:
- Increasing complexity of the advanced semiconductor package technology
- Battery capacity expansion
- Antenna integration and placement

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PCB Design and Fabrication Trends – Automotive

<table>
<thead>
<tr>
<th>Diversity – Functionality – Complexity – Miniaturization - Connectivity</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ADAS/Automated Driving</strong></td>
</tr>
<tr>
<td>Now 77 – 81GHz, Next Gen up to 140GHz</td>
</tr>
<tr>
<td>Cu surface</td>
</tr>
<tr>
<td>Hybrid stack-up</td>
</tr>
<tr>
<td>HDI (≤0.4mm) &amp; anylayer technologies</td>
</tr>
</tbody>
</table>

| **Electrification** |
| A few 100A and 400/800/1200Vdc |
| Heavy Cu |
| Standard HDI |
| CAF |

| **Digitalization/Infotainment** |
| 25/56Gbps (13/28GHz) |
| ≤0.4mm pitch |
| Advanced HDI technology |
| New Surface finishes |

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**Material Technology**

**RELIABILITY**
- Harsh environment
- Longer T/H/B impact (>100000hrs)
- Space between conductors (e.g. CAF)
- Increasing temperature load (up to 170C) and hotspots
- High voltage CAF testing (+1000V)

**THERMAL MANAGEMENT**
- Increasing temperature load (up to 170C) and hotspots
- Local anisotropic heating e.g. power lines.
- EV power train high voltage electronics
- Smaller feature size (hot spots)
Speaker Introduction

Dr. Gokul Kumar
Sr. Manager, Packaging Design and Development
Micron
Speaker Introduction

Dr. Min Woo (Daniel) Rhee
Program Manager
R&D
Samsung Electronics
- Panel Session -

Packaging Challenges & Opportunities for 5G applications

Minwoo Rhee, Ph.D, MOT
Manufacturing Technology R&D Center
Samsung Electronics
5G : Challenges & Opportunities

5G mmWave – New Paradigm Shift

• 5G NR (below 6GHz & 24~100GHz), above 20 times faster than 4G with few ms delay
• Next platform for smartphone, IoT, Autonomous vehicle
• R&D expenditure and new equipment investment is increasing (10 times higher than LTE)
• New system, device, packaging, module design, materials and testing - The winner takes all

Commercialization Status:
- KT (S. Korea): Announced (Oct’19) 28GHz base 5G system improved delay from 20ms (3.5GHz) to < 5ms
- Verizon (US): began offering 5G WiGig (Oct’19) to replace home wifi with 5G NR transmission standard and equipment
5G : Challenges & Opportunities

- Above 24GHz mmW, the signal is closer to light and it is difficult to get over the obstructions such as mountains and buildings with limited coverage (~200m)
- To overcome this, 5G NR needs Massive MIMO and beamforming for individual smartphone

4G LTE Base Station to Cell
- One-way spot lighting
- Multiple users per cell
- 4x4 Antenna Array
- 16 Antenna Connections
- Active Antenna System

5G NR Base Station to Cell
- Both-way spot lighting
- User by user beamforming (MIMO processing)
- 8x8 Antenna Array
- 64 Antenna Connections
- Massive MIMO System
- Single adaptive cell

Source : Xilinx
As a result, to realize the beamforming and MIMO for 5G NR, the number of the antenna needs to be increased. Conventional LDS (Laser direct structuring) antenna has design limitations.

To overcome this, 5G NR needs a Beamforming Antenna Module Array with Package level integration.

**4G LTE LDS Antenna**

- Maximum No. of Antenna: 4

**5G NR 8x8 MIMO Phase Array Antenna**

- Need more Antenna with Isolation spacing

**BF Antenna Module**

- How?
  - FPCB+RFIC?
  - SMD?
  - Dielectrics (FR4) or LTCC/Glass?
  - Design?
  - Interconnection?
  - Patterning?
  - Signal Processing Algorithm?
  - META materials?
5G Packaging Challenges

- More RF contents need expertise (mmWave)
- Requires new materials of low-k low-loss tangent
- Highly integrated MCM or SiP solutions required for 5G packaging
- Antenna in Package (AiP)
- More analog conversion to advanced packaging such as WLP
- Industry 4.0 should be employed for SiP manufacturing line

(source: SW Yoon Semicon Korea 2019)
5G Test Challenges

- Test platform is also new
- Requires new Capex for investment
- More RF contents need expertise
- mmWave testing requires specific knowledge and expertise
- Different applications may lead to new set of testers: short longevity
- Contact or OTA? Industry still remain undecided
- How to deal with cost and parallelism?
- In order to support high signal integrity, measurement errors such as impedance mismatch, cable loss, and RF source variation over time become important at mmWave ranges

(source: New test methodologies for 5G wafer high-volume production By Daniel Bock, Jeff Damm [FormFactor, Inc.]. Chip Scale Review 2019 Jan-Feb)
Thank you for your attention!

Legal Disclaimer

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Panel Session:
Packaging challenges & opportunities
for 5G applications

Please tell your name and company before your question.
Thanks!
Panel Discussion:

What are the major differences as to the materials or package types used among different applications, such as high-speed computing, network infrastructure, automotive compared with smart phones?

What role do you expect ceramic, organic, silicon, and glass substrate to play in 5G mmWave applications?

5G mmWave antenna and RF-front end module require high integration, what are the major issues from the material or packaging perspective?

As to manufacturing, will the adoption of new materials and packages used in 5G cause the capability challenges to the equipment or assembly processes? If so, what are the challenges the industry should overcome?

What are the major measurement and test challenges for 30-60GHz or even higher? At PCB or package level, or at the module or product level?

Any comments or suggestion to industry collaboration? Would a consortia effort for common test coupon(s) and test guideline development be needed?