1st Level Interconnect Void Characterization Project

Project chair: Kor Oon Lee/ Intel
Co-chair: Sze Pei Lim/ Indium
Kiyoshi Ooi/ Shinko

Webinar recording:
https://inemi.webex.com/inemi/lsr.php?RCID=ccbecf1bb9644703bcafa0afa391314f

(this link is good for up to six months following the webinar)

Call for Participation Webinar
December 12, 2019
iNEMI Staff: Masahiro Tsuriya
Agenda

• Introduction of Project Chairs and Facilitators
• iNEMI Project Development Process
• Project Briefing
  – Background & Objectives
  – Project Scope
  – Project IS/IS Not
  – Two Phased Projects Outline
  – Timeline
• How to Join
• Q&A

Note: All phones will be on mute until the end of the presentation
Project Chairs and Facilitator

Project Leader:
Lee Kor Oon (Intel)

Project Co-Leader:
Sze Pei Lim (Indium)

Project Co-Leader:
Kiyoshi Ooi (Shinko)

iNEMI Staff:
M. Tsuriya
iNEMI Project Development Process - 5 Steps

0. INPUT

1. SELECTION

2. DEFINITION

3. PLANNING

4. EXECUTION / REVIEW

5. CLOSURE

“Initiative” Open for Industry input

-------------------
iNEMI Technical Committee (TC) Approval Required for Execution

“Project” Limited to committed Members
Project Briefing
Electronic Packaging Trend

- SIP
- DIP
- QFP
- CLCC
- PLCC
- FCBGA
- MCP
- PoP
- FCCSP
- 2.5D IC
- 3D IC
- Modular chiplet design
- Intel Foveros, EMIB

 Scaling down of feature size

1970 - 2020

No of transistors, I/O count, functionality

Shrinking bump size
Flip Chip Bump - challenges

• The formation of small voids (micro voids) can occur in solder-based flip chip joints during the assembly process

• Void within flip chip tends to grow especially after multiple reflow (solid-liquid-solid)
  • This can be a concern for certain applications that involve high electrical and thermal flux across the flip chip
  • The void formation can have an impact on electromigration in the joint. The presence of a void can accelerate the complete open failure due to electromigration

• X-ray is the preferred method of inspection for voids; however, it is challenging to accurately locate and measure the size of the voids or percentage of voiding due to the small dimension of the flip chip bond and the interference of substrate and die metallization.

• There are no guidelines or standards presently which define an acceptable percentage of voiding or how the percentage of voiding relates to the reliability of the assembly.

Voids in first level interconnect materials have the potential to impact adversely on reliability of electrical interconnect, particularly as a result of, electromigration. Through the project, this project will

- Study the inspection capability of micro-void in the flip chip bump
- Perform experimentation to understand the relationship between void and the joints reliability (electrical and Mechanical)
- Strive to develop recommendations for the industry and standards bodies on the acceptable voiding characteristics for flip chip interconnects for the required packaging reliability.
### IS/ IS NOT Analysis

<table>
<thead>
<tr>
<th>This Project IS:</th>
<th>This Project IS NOT:</th>
</tr>
</thead>
<tbody>
<tr>
<td>To study the impact of solder voids on package reliability</td>
<td>Develop new soldering/ joining material and process</td>
</tr>
<tr>
<td>Study the failure modes for first level interconnect materials, particularly those driven by electromigration.</td>
<td>Establish the inspection methodology of voids</td>
</tr>
<tr>
<td>Understand the inspection/methodology capability limitations for micro voids</td>
<td>Development of a specific standard(s)</td>
</tr>
<tr>
<td>Assess the reliability risk of voids location</td>
<td>Repeat of prior or existing work</td>
</tr>
<tr>
<td></td>
<td>Biased towards specific suppliers, geographies, or market segments</td>
</tr>
</tbody>
</table>
The project will have 2 distinct phases:

- **Phase 1:**
  - Study and determine the inspection capability of micro-voids in first level interconnect materials
- **Phase 2:**
  - Study the relationship between voids and the electrical and mechanical reliability of the assembly
Phase 1
X-ray Measurement Capability Study

- **Test Vehicle Build**
  - **Material Sourcing:**
    - Substrate (dummy substrate should be okay)
    - Micro Solder Balls (ball size and solder composition to be determined by the team)
  - Micro Balls attached on the substrate by manual process

- **Void Inspection**
  - X-ray equipment is used to measure voids on as-is TV sample (no reliability testing performed)
  - X-sectioning of micro balls and measure the voids by SEM/ FIB

- **Data Analysis**
  - Project Phase 1 Summary reporting
  - Judge Go/NO GO to next step
  - Phase 2 experiment outline proposal
Phase 2
Voids to Electrical/Mechanical Reliability Study

- Design of Experiment
  - Develop the testing system to find the relationship between voids vs. electrical/mechanical reliability
  - Determine the material selections for the DOE
  - Decide on sample sizes of each Flip Chip BGA package types (either or both of C4 balls and Cu pillar with solder paste)

- Material Sourcing
  - BGA substrate sourcing
  - Test board sourcing
  - Test Die (daisy chain) sourcing

- Test Vehicle Build (Flip Chip Packages Assembly)
  - Cu pillar fabrication on daisy chain dies and Solder plate on Cu pillar (as needed)
  - Flip Chip attach to substrate (both C4 solders or Cu pillar interconnect)
  - Board assembly to the test boards

- Testing and Data Collection
  - Void Inspection before/after tests
  - Reliability Test:
  - Electrical testing: Resistance checks
  - Failure Analysis:

- Data Analysis and Report Writing, and Webinar
DoE – Phase 2
Note: When phase 1 will be completed, this DoE will be reviewed and determined by the team.

<table>
<thead>
<tr>
<th>Tasks</th>
<th>Resource type</th>
<th>Contributing firm</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Vehicle</td>
<td>Flip Chip Substrate</td>
<td></td>
<td>Standard design is used.</td>
</tr>
<tr>
<td></td>
<td>Underfill</td>
<td></td>
<td>Standard material is used. (only 1 type)</td>
</tr>
<tr>
<td></td>
<td>Flip Chip Bump</td>
<td></td>
<td>Micro ball, plating</td>
</tr>
<tr>
<td></td>
<td>Cu pillar build on dies</td>
<td></td>
<td>Option</td>
</tr>
<tr>
<td></td>
<td>Silicon Die (daisy chain)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Flip Chip BGA Assembly</td>
<td></td>
<td>Not required to use the qualified assembly line</td>
</tr>
<tr>
<td>Test Board</td>
<td>Rigid Test Board Design</td>
<td></td>
<td>Allow for in situ monitoring during testing (resistance checks)</td>
</tr>
<tr>
<td></td>
<td>PCB Fabrication</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Test Board Assembly</td>
<td>Board Assembly</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Void Inspection</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Test</td>
<td>ATC</td>
<td></td>
<td>-55/125°C (condition B), 1000 cycles (either one of ATC or TS)</td>
</tr>
<tr>
<td></td>
<td>TS</td>
<td></td>
<td>-40/125°C with ramp rate &gt;20°C/min (either one of ATC or TS)</td>
</tr>
<tr>
<td></td>
<td>Resistance Measurement</td>
<td></td>
<td>In-situ</td>
</tr>
<tr>
<td></td>
<td>Void Inspection</td>
<td></td>
<td>After ATC/TS test</td>
</tr>
<tr>
<td>Electrical Test</td>
<td>Electro-migration test</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Failure Analysis</td>
<td>Failure Analysis</td>
<td></td>
<td>optical metallography, polarized light microscopy, and scanning electron microscopy</td>
</tr>
<tr>
<td>Phase 1</td>
<td>Q1</td>
<td>Q2</td>
<td>Q3</td>
</tr>
<tr>
<td>--------------</td>
<td>----</td>
<td>----</td>
<td>----</td>
</tr>
<tr>
<td>Task 1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Task 2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Task 3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Task 4</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Phase 2</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
<th>Q5</th>
<th>Q6</th>
<th>Q7</th>
<th>Q8</th>
<th>Q9</th>
</tr>
</thead>
<tbody>
<tr>
<td>Task 5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Task 6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Task 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Task 8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Task 9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Task 10</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: Schedule with Milestones will be reviewed at the kick-off meeting.
How To Join
iNEMI Project Management Policy

• Two governing documents for projects
  – SOW (statement of work):
    sets out project scope, background, purpose, benefits, and outlines
    required resources, materials, processes, project schedule, etc.
  – Project Statement (PS):
    signed by participating companies to secure commitment on resource
    and time contributions.

• iNEMI Project requires iNEMI membership
  – Signed membership agreement
  – Commitment to follow iNEMI By-laws and IP policy
Sign-Up Due on January 31, 2020

- iNEMI membership is required to join the project
- Download SOW and PS from iNEMI web:
  https://community.inemi.org/1st_level_interconnect_void_characterization
- Process to participate this project:
  - Sign the PS
  - Send scanned PS to infohelp@inemi.org
  - iNEMI VP of Operations will approve your participation and send you back the completed PS with acceptance
- Join iNEMI membership, or questions, contact M. Tsuriya (m.tsuriya@inemi.org)
Path to Kick-off Meeting

• Call for Participation Webinar: December 12, 2019
• Sign-up Due: by January 31, 2020
• Kick-off Meeting:
  
  February 7(Fri), 2020 from 10:00a.m. Japan time
  
  February 6 (Thu), 2020 from 21:00p.m. Japan time

Note:

Meeting time might be changed due to the participants’ preference and availability
Questions?

Project web page:
https://community.inemi.org/1st_level_interconnect_void_characterization