iNEMI Substrate & Package Technology Workshop
Agenda and Speaker Bios/Abstracts

Where:
IBM Singapore Office
6 Tampines Industrial Avenue 5, Singapore 528760

When:
May 26 (full day) and 27 (half day), 2016

What you will earn:
The purpose of this workshop is to assess advanced substrate and package technology capabilities and gaps, including fan-out WLP and 3D-IC with/without TSV, and SiP substrates. Experts from the electronics manufacturing supply chain will present their expertise on materials, equipment, assembly processes and package systems from the users’ requirements. Attendees will have the opportunity to debate key questions at the second day during break-out sessions.

Workshop Program:
Day 1:
8:15: Registration starts
9:00 – 18:00: 12 presentations from the technology experts

Day 2:
8:15: Welcome Coffee
8:30 – 12:45: Breakout Session and Wrap-up

Registration:
Click here to register.

<table>
<thead>
<tr>
<th>iNEMI Member</th>
<th>Non-Member</th>
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<td>$250 (USD)</td>
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The registration fee covers participation in the workshop and access to the presentation documents. Light beverages are provided during the workshop breaks on both days.

Refund Policy:
A full refund will be given for cancellations until April 20, 2016. After April 21, no refunds will be given.
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<td>Registration Start</td>
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<td>09:00 – 09:10</td>
<td>Welcome Speech</td>
<td>Annie Wong</td>
<td>GM, IBM Manufacturing Solutions, Singapore</td>
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<td>09:10 – 09:30</td>
<td>iNEMI Introduction</td>
<td>Haley Fu</td>
<td>Managing Director, iNEMI</td>
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<td>09:30 ~ 10:15</td>
<td>An Overview of Market and Technology trends in the Advanced Packaging ecosystem</td>
<td>Santosh KUMAR</td>
<td>Sr Analyst, Yole Development</td>
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<td>10:15 ~ 10:30</td>
<td>Tea and coffee break</td>
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<td>10:30 ~ 11:00</td>
<td>Package Scaling and heterogeneous integration</td>
<td>Wei Keat Loh</td>
<td>Sr Technology Development Engineering Manager, ATTD, Intel</td>
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<td>11:00 ~ 11:30</td>
<td>Solder Alloy Options for the Semiconductor and PCB Assembly</td>
<td>Sze Pei Lim</td>
<td>Regional Product Manager – Semiconductor, Indium Corp.</td>
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<tr>
<td>11:30 ~ 12:00</td>
<td>Device Embedded Package MCeP for SiP application</td>
<td>Tetsuya Koyama</td>
<td>Manager of Interconnect Technology Development, Shinko</td>
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<td>12:00 ~ 12:30</td>
<td>Wafer/Panel Level Encapsulation - an Alternative Format for Plastic Packaging: Its Challenges and Solutions</td>
<td>Eric Kuah</td>
<td>VP, Technology Encapsulation Solutions Group, ASM Singapore</td>
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<td>12:30 – 13:15</td>
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<td>13:15 ~ 14:00</td>
<td>An End User’s Perspective on Qualifying New Packaging Technologies</td>
<td>Curtis Grosskopf</td>
<td>Senior Engineer, System Supply Chain Engineering, IBM</td>
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<td>14:00 ~ 14:30</td>
<td>eWLB /FO-WLP : Present and Future of Advanced Wafer Level Packaging Technology</td>
<td>SW Yoon,</td>
<td>Director / Products &amp; Technology Marketing, STATSChipPAC</td>
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<td>14:30 ~ 15:00</td>
<td>Advanced substrate materials for next generation low CTE/thinner package with high reliability</td>
<td>Hiroaki Fujita</td>
<td>Hitachi Chemical</td>
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<td>15:30 ~ 16:00</td>
<td>SiP in NXP</td>
<td>L.C. Tan,</td>
<td>Head, Assembly Process Innovation NXP Semiconductors</td>
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<td>16:00 ~ 16:30</td>
<td>High End Organic Substrate Direction</td>
<td>Koichi Nonomura</td>
<td>Manager of FCBGA Product Engineering, KYOCERA</td>
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<td>16:30 ~ 17:00</td>
<td>Stanley Wu</td>
<td>Technical Manager, ASE</td>
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<td>Innovative SiP Technology</td>
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<td>17:00 ~ 17:45</td>
<td>Surya Bhattacharya</td>
<td>Director, A*STAR Institute of Microelectronics (IME)</td>
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<td>Heterogeneous Integration Platforms for Mobile and IoT</td>
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<td>17:45 ~ 18:00</td>
<td>Day 1 Wrap-up</td>
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May 27, 2016

08:15  Welcome Coffee

08:30 – 12:45: Breakout Session and Wrap-up

08:15  Welcome Coffee

08:30 – 12:45  Breakout Session and Wrap-up
Santosh Kumar, Sr. Analyst
Yole Development

Santosh Kumar is working as Senior Technology & Market Research Analyst at Yole Développement where he is involved in the market, technology and strategic analysis of the microelectronic assembly and packaging technologies.

He received the bachelor and master degree in engineering from the Indian Institute of Technology (IIT), Roorkee and University of Seoul respectively. He has published more than 30 papers in peer reviewed journals and has obtained 2 patents. He has presented and given talks at numerous conferences and technical symposiums related to advanced microelectronics packaging.

**Title: Overview of Market and Technology trends in the Advanced Packaging ecosystem**

**Abstract:**

Semiconductor industry has entered a new era where the cost to design and manufacture devices at advanced node (14nm and beyond) is not bringing desired cost benefits as predicted by Moore’s law. In order to answer market demands, the industry seeks further performance and functionality boosts in integration. While scaling options remain uncertain and continue to be investigated, the spotlight is turning to advanced packages. Emerging packages such as fan-out wafer level packages and 2.5D / 3D IC solutions together with upgraded flip chip BGAs aim to revive the cost/performance curve and extend both scaling and functionality roadmaps. This presentation will give an overview of the market and technology trends of the advanced packaging ecosystem including market forecast, new applications and supply chain.
Loh Wei Keat (PhD) is the Senior Technology Development Engineering Manager in Assembly Technology and Test Development (ATTD) in Malaysia. Wei Keat manages the Thermal, Mechanical and Fluid core competency team that focuses on simulation technology to define next generation package design, enhance solder joint reliability, packaging level reliability, package warpage as well as assembly related mechanical-thermal-fluid flow interaction prediction capability for supporting high volume manufacturing of advance electronics packages. Wei Keat has contributed to multiple packaging technologies during his 13 years tenure with Intel. Wei Keat is currently leading the “Warpage Characteristics of Organic Packages Phase 3” in one of the iNEMI project roadmaps. Wei Keat obtained his PhD from University of Surrey, UK; specialized in fracture mechanics and predictive modeling. Wei Keat has published more than 45 papers and holds two patents in electronics packaging related research. During his free time, Wei Keat enjoys working on drones, building 3D printer and car maintenance projects.

**Title: Package Scaling and heterogeneous integration**

**Abstract:**

Industrial community continue to develop more advanced semiconductor packaging technologies that continue to enable progress and growth in the evolution of smart and connected devices. This presentation talks about the technological trends and drivers of advanced packaging research, and discusses the challenges and opportunities driven by application specific requirements. The first level interconnect (chip to package) and the second level interconnect (package to board) pitch scaling are the essential to decrease the gap with the relentless silicon technology scaling. Increasing bandwidth density within the package drives innovation including logic and memory interconnects with 2D, 2.5D and 3D integration. System densification in Wearable/IoT drives innovations in on-package integration / System-in-Packaging technology, Low Cost Flip Chip / Wafer Level Packaging technology to enable further reduction in cost, size and power. Meeting the push for ultra-thin form factors will require advances in thin wafer handling, thin die assembly, thin substrate manufacturing, and package warpage controls. With scaling packaging design rule continues, the sensitivity to smaller defect increase significantly and impact to the metrology / Inspection system. The objective of this presentation is to communicate industry challenges and to encourage the audience to engage in collaborative development efforts to solve these issues.
Sze Pei LIM, Regional Product Manager - Semiconductor

Indium Corporation

Sze Pei Lim is the Regional Product Manager for Semiconductor Material and is based in Malaysia. She manages the Semiconductor product lines for the whole of Asia region. Working closely with the local Sales team, understanding customers' needs and requirement in the semiconductor industries, she then communicate with R&D team and offer timely solutions to the customers.

Sze Pei joined Indium Corporation in 2007. Before taking up her current role, she was the Technical Manager who managed the Technical Support team in South-East-Asia. Prior to joining Indium, she was a research and development chemist. Her research included solder paste and flux formulation. She also worked as a technical manager for nine years for Inventec, where she provided technical support and managed testing in the lab.

Sze Pei has over 25 years of experience, mainly in the areas of PCB assembly and surface mount technology. She earned her bachelor’s degree from the National University of Singapore, majoring in industrial chemistry with a focus in polymers. Sze Pei is a SMTA-certified Process Engineer and has earned her Six Sigma Green Belt.

Title: Solder Alloy Options for the Semiconductor and PCB Assembly

Abstract:

Even though Sn96.5Ag3Cu0.5 (SAC305) is being used as the mainstream alloys for at least the past 3-4 decades, but in recent years, the industry is facing more challenging technology that the use of SAC305 has encountered some limitations. The warpage issue of thin packages, is driving the industry to look into alloys with lower melting point than SAC305, and yet having the malleability of Sn63Pb37. Besides, this lower melting alloy can be used for heat sensitive devices and save some energy cost at the same time. On the other hand, the demanding operating condition for the automotive under-the-hood application, has driven some companies to look into other Pb-free alloys that can achieve better reliability performance than SAC305. This presentation will discuss and share some of the other Pb-free solder alloy options for the different industry and applications.
Tetsuya Koyama, Manager of Interconnect Technology Development Dept. R&D Div.

Shinko Electric Industries Co., LTD.

Tetsuya Koyama received B.E. and M.E. degrees from Waseda University, Tokyo, Japan. He joined Shinko Electric Industries in 1991 and he has over 25 years’ experience of new semiconductor package development. He is interested in new package structure and new materials for semiconductor package.

**Title: Device Embedded Package MCeP for SiP Application**

**Abstract:**

Along with miniaturization and high functionality of portable mobile device, small form factor semiconductor package has been required. Many new packages have been investigated. WLP and device embedded packages were developed and become to commercial volume production.

As the device embedded package, Shinko has been developing Molded Core embedded Package, MCeP. MCeP consists of base substrate, upper substrate and molding resin. Bare IC device without rerouting is mounted on top surface of base substrate by flip chip bonding. Base substrate and upper substrate are connected electrically by copper core solder balls. The space between base substrate and upper substrate is encapsulated by molding resin.

MCeP structure is possible to reduce package size and maintain small warpage.

For the future MCeP, smaller package size and thinner package height are desired. For small form factor, finer connection pitch between base and upper substrate is necessary. Current design rule of the connection pitch is 0.300mm, but in the future, it will be shrunk to 0.200mm and 0.150mm. Instead of copper core solder ball, copper pillar connection has been investigated. It will be easily achieved finer interconnection pitch. On the other hand, for thinner MCeP, thinner substrates will be applied.

Application of MCeP is not only single die package, but also SiP module with multi die embedded. For SiP module application, assembly technology, for example, multi die flip chip, passive components embedded and finer trace fabrication substrate technology have been investigated. Less than 0.150mm thickness components were embedded in MCeP and measured electrical characteristics. It showed better electrical performance compared with no passive components embedded module. For finer pitch substrate, Shinko developed integrated Thin film High density Organic Package, i-THOP. Design rule is L/S=0.002/0.002mm and via diameter = 0.010mm.

Demonstration sample of MCeP structure with i-THOP base substrate was fabricated. It showed that MCeP had potential structure to be applied to multi die embedded module.

In conclusion, MCeP was developed as PoP bottom package application. In the future, MCeP will be also applied SiP module with multi die embedded with passive components using finer pitch substrate, i-THOP.
**Title: Wafer/Panel Level Encapsulation - an Alternative Format for Plastic Packaging**

The plastic package production is a very sizeable market, offering many different packages for a variety of applications such as ESD protection, MOSFETS among others. The current packaging and assembly methodologies use leadframe to produce packages such as DSN, DFN, SOD, QFN, BGA and SOT. The advent of producing these packages on either the wafer or panel level format has arrived. In our recent packaging and assembly work we found that producing discrete package using wafer level format is feasible from the perspective of cost of production and technology. From the viewpoint of cost production, a significant portion of the manufacturing process can be eliminated, for instance interconnected technologies using wire bonding. This will translate into a reduction in cost of production and an increased throughput. In the aspect of technology, power efficiency can be further improved. The focus of our presentation is to share our experience in producing such plastic package, and in particular encapsulation. We will discuss the challenges and solutions that a packaging/equipment engineer will face during the molding process of these discrete packages at a wafer/panel level. Technical solutions to be discussed are material handling, encapsulation tool design, encapsulant selection, warpage control, voiding, and moldability solutions. Silicon wafer that allows one to produce it as either a 5S (five-sided package) or 6S (six-sided package) discrete package.
Curtis Grosskopf, Senior Engineer for IBM in System Supply Chain (SSC) Engineering.

IBM Corp.

Curtis Grosskopf has 28 years of experience in IC packaging and the interaction of IC packages with electronic card assembly, with emphasis on moisture sensitivity and process/temperature sensitivity issues. Technical lead for the component procurement team within IBM for environmental (RoHS, REACH, etc.) and Pb-free issues. Actively participated in industry standards generation for 26 years, initially with the release of IPC-786 (Moisture Sensitivity) and still with J-STD-020 in the B-10a working group, to also now chairing IPC 2-15f working group for Product Discontinuance and Product Change Notices. Has been chairman of the JEDEC JC14.4 Quality Processes and Methods committee for the past 9 years and active participation in JC14.1, 14.3, and 14.4 committees since 2003. Graduated from the University of Wisconsin - Madison with a BS and MS in Engineering Mechanics.

Title: An End User's Perspective on Qualification of New Packaging Technologies

As a manufacturer of high reliability computing and storage systems, IBM’s goal in qualifying IC packages and card assemblies is to ensure that they meet our high expectations for initial quality and long term reliability, support our overall system electrical and thermal performance targets, and help to reduce the overall cost of our systems. IBM's mainframe computers are called “Z” systems. The “Z” stands for Zero downtime, which is what our customers expect from the mainframe. These systems are used by banks, airlines, and other companies/organizations who cannot accept their mainframe to ever go down. These systems have multiple layers of redundancy, however, they still require fully qualified, high reliable devices.

Gone are the days of IBM’s thermal conduction modules (TCMs) with ceramic substrates and flip chip bipolar chips. Gone too are the days when IBM designed the package and assembled all of its ICs and assembled those devices onto its cards in IBM assembly facilities. Today, IBM relies on its suppliers (and their supply chain) to develop and qualify most of the products used within its high end systems. These include devices with stacked die, leading edge silicon and packaging technology, and complex modules with densely packed ICs and passives that to a novice, looks like a packaged monolithic IC. The problem with this is that these complex devices and modules rarely respond to card assembly stresses in the same manner as simple monolithic ICs. For this presentation IBM would like to highlight a few areas that its wants the electronics industry (electronic component suppliers, component subcontract assemblers, material suppliers, module designers, and card assemblers) to include in their design, manufacturing, and qualification processes as it develops and offers these new packaging and integration solutions. Some of the more important points that will be discussed include:

- understand fully the end user's assembly processes and system use conditions;
- be aware of the benefits of test vehicles in the qualification process;
- as packages become more complex it becomes more necessary to understand the stresses and potential fail modes within new packages;
- there must be a constant focus on quality even though reducing cost and speed to market drive everything;
- even with new technology there is a need to share key information early for the development/improvement of industry qualification standards and test methods; and
- as new packages and processes are developed, don’t reintroduce old quality and reliability issues.
Seung Wook Yoon, Ph.D, Director / Products & Technology Marketing

STATS ChipPAC, JCET Group

Dr. YOON is currently working for Products & Technology Marketing in STATS CHIPPAC LTD. His major interests are for wafer level products including eWLB/Fanout WLP, WLCSP, IPD (integrated Passive Device), flipchip bumping, TSV (Through Silicon Via), SiP and integrated 3D IC packaging.

Prior to joining STATS CHIPPAC LTD, He was deputy lab director of MMC (Microsystem, Module and Components) lab, IME (Institute of Microelectronics), A*STAR (Agency of Singapore Technology and Research), Singapore. "YOON” received Ph.D degree in Materials Science and Engineering from KAIST, Korea. He also holds MBA degree from Nanyang Business School, Singapore. He has over 250 journal papers, conference papers and trade journal papers, and over 25 US patents on microelectronic materials and electronic packaging. Currently contributing as technical committee member of prestigious international conferences, such as EPTC, ESTC, iMAPS, IWLPC and SEMI.

Title: eWLB /FO-WLP: Present and Future of Advanced Wafer Level Packaging Technology

ABSTRACT

The number of WLCSP (Wafer Level Packages) used in semiconductor packaging has experienced significant growth since its introduction in 1998. The growth has been driven primarily by mobile consumer products because of the small form factor and high performance enabled in the package design. And it is also attractive to WE (wearable electronics) and IoT (Internet of Things) products. Although WLCSP is now a widely accepted package option, the initial acceptance of WLCSP was limited by concerns with the SMT assembly process and the fragile nature of the exposed silicon inherent in the package design. Assembly skills and methods have improved since the introduction of the package, however damage to the silicon remains a concern. The side or top of the die continue to be exposed after dicing the wafer and the silicon continues to be at risk for chipping, cracking, and other handling damage during the assembly process.

This paper introduces eWLB (embedded Wafer Level Ball Grid Array) /FO-WLP (fanout –WLP) for its improved and advanced reliability. In these new packages EMC is applied to all exposed silicon surfaces on the die. The manufacturing process leverages existing high volume manufacturing methods with exceptionally high process yields. eWLB is a type of FO-WLP that has the potential to realize any number of interconnects with standard pitches at any shrink stage of the wafer node technology. This paper also discusses the wide range of FOWLP/eWLB adoptions and new features available for emerging market of IoT and WE. This advanced technology is well designed for 3D PoP, MEMS/sensors, 3D SiP modules as well as ultra-thin, highly integrated packaging solutions. Innovative FOWLP/eWLB features are also introduced with the merits and thermal/electrical characterization data as well as reliability test results.
Hiroaki Fujita, Ph.D., Staff Researcher / Laminate Materials R&D Dept.
Hitachi Chemical Co., Ltd

Dr. Fujita is currently working for electronics-related materials development center in Hitachi Chemical Co., Ltd. His major interests are laminate materials for thinner/high-density PKG and FC-BGA, Packaging technologies with high reliability.

He received the Ph.D. degree in material science from JAIST, Japan. He joined Hitachi Chemical Ltd., Japan, as a printed wiring materials development engineer. The second, he joined Telecommunication Materials Development Center with Research Laboratory, where he was involved in the analysis of packaging assemblies, warpage mechanisms and connection reliability. His current researches include the advanced laminate materials for integrated 3D IC package.

**Title:** Advanced substrate materials for next generation low CTE/thinner package with high reliability

**ABSTRACT**

Currently, with increasing demand for smart phones and tablet computers, further high-volume, high speed, low power consumption LSIs and smaller/thinner semiconductor PKG are strongly required. The semiconductor PKG substrate installed in these devices is demanded to be thinner and higher in density. As one of the most innovative solutions, the PoP (package on package) technology, capable of stacking different IC packages such as memory and logic, has been expanding. However, thinner PKG such as PoP tends to warp at the assembly process and cause the decrease in the connection reliability. Therefore, low CTE (coefficient of thermal expansion) core materials have been needed as a key solution for the reduction of the warpage for PoP. To meet this requirement, we have been developed low CTE core material and confirmed that not only low CTE but also low resin shrinkage gave big impact to the warpage.

In this paper, we would like to introduce new resin system for low CTE core material aimed at thinner PKG. At the same time, we would like to explain the relationship between the warpage and material property. New resin system which shows smaller warpage was achieved by optimizing stacking structure between suitable aromatic units. The intermolecular interaction between them would lead to low CTE and low shrinkage. In order to achieve further low CTE and shrinkage, we attempted introducing low elastic component into the resin system. It was suggested that compatibility of the low elastic component was important factor from molecular simulation. By the reduction of free volume optimizing intermolecular interaction between the low elastic components in the resin, ultra-low CTE and low shrinkage were achieved. Finally, we confirmed that not only ultra-low CTE but also low shrinkage of core material contributes to the decrease of thin PKG warpage effectively.
LC, Tan, Head, Assembly Process Innovation

NXP Semiconductors

LC Tan has been in the semiconductor industry for over 26 years with a wide ranging experience in various packaging technologies development and introduction. She holds a master degree in semiconductor packaging technology as well as MBA. LC has 21 issued patents to-date and is currently a Regional Manager for Assembly Package Innovation in NXP’s Global Technology Innovation group.

Title: SiP in NXP

An introduction of NXP’s latest single chip system module technology will be made in this presentation detailing some of the key miniaturization enablers.
Koichi Nonomura, Manager of FCBGA Product Engineering Section, Ayabe Plant

KYOCERA, Inc.

Koichi Nonomura was received the bachelor degrees in electronics from Nihon University Japan in 1984. And had some company carrier in electronics design and engineering through IBM to KYOCERA for 31 years. I am now in charge of flip chip organic product engineering manager and focus on 2.5/2.1D. Today, I will talk about high end organic substrate direction.

Title: High End Organic Substrate Direction

Abstract:

By enhancement of cloud computing system, WEB internet access of higher speed and data is continuously demanding, going to beyond 400G ether net access, and expecting market growth to deliver 8K 3D video data on line. So that application of semiconductor is followed that way and needed more logic circuit integration with narrow gate length wafer. Meantime, such high end is requiring and need the enhancement, so KYOCERA is developing the structure with higher pin count and speed support. The substrate technology needs is low electrical loss and low physical expansion, but the organic substrate has a challenge to maintain insulator resin system. For next generation device node, we developed low dielectric loss material and low conductive loss process. However, further more future, we need to work with higher system level design. And one of proposal is to integrate high speed memory die on organic substrate like 2.5D / 2.1D packaging. In this session, introduce APX and discuss for high end substrate direction and system level innovation.
**Stanley Wu**, Technical Manager

**ASE Group**

**Stanley Wu** is currently as Technical Manager of ASE Group in Singapore sales office. He has over 10 years of package design and solution in the field of IC packaging. In 2005, he joined ASE in Kaohsiung, Taiwan and responsible for substrate design for both wire bond and flip chip package. Also, he works in customer engineering integration team and in charge of project management and product development which applies various package solutions including bumping, WLCSP, Leadframe/Substrate based package and SiP. Currently, he focus on package solution providing and promotion especially for System in Package and also module assembly.

Stanley Wu has received the Electrical Engineering BS from Chung Yuan Christian University in Taiwan.

**Title: Innovative SiP Technology**

**Abstract:**

Humanisation is driving SiP integration. New and proven SiP technologies and solution are available today. Integration of SiP technologies can enable performance, form factor and development cost requirements of the next generation of electronic devices.
Dr. Surya Bhattacharya, Director of Industry Development, Interconnect Packaging & TSV Programmes

A*STAR Institute of Microelectronics (IME)

Dr. Surya Bhattacharya is Director, Industry Development, for IME's Through Si Interposer (TSI) and High Density Fan-Out WLP Programs. Surya has over 20 years of experience ranging from 0.8micron to 28nanometer CMOS while working in the US semiconductor industry at both Fabless companies and Integrated Device Manufacturers (IDM). He joined IME from Qualcomm CDMA Technologies, San Diego, California, a world leader in semiconductor chips for 3G and LTE mobile phone markets. At Qualcomm, he served as Director of Foundry Engineering while he oversaw technology and manufacturing ramps across multiple foundries in Asia and around the world. Prior to Qualcomm, he was a Principal Foundry Engineer at Broadcom Corporation, Irvine, California, driving CMOS development and manufacturing for Broadcom's networking and wireless products at Asian foundries. He started his career at Rockwell Semiconductor Systems, Newport Beach, California, where he was Senior Manager for CMOS technology development for Rockwell's communication products. Surya obtained his Bachelor of Technology degree in Electrical Eng from the Indian Institute of Technology Madras, India in 1987; MS, and Ph.D Degree in Microelectronics from the University of Texas at Austin, Texas, USA in 1993.

Title: Heterogeneous Integration Platforms for Mobile and IoT

Mobile Devices and The Internet of Things (IoT) have led to unprecedented demands in terms of data-traffic. Data-sharing networks need to be capable of storing and transmitting large amount of data as well as perform smart data-analysis to enable timely planning and decision-making in both personal (e.g. social, health) and enterprise (e.g. business, factory, traffic management) settings. To handle rapidly increasing amount of data, microelectronic devices and the interconnects between the vast number of devices within smaller systems (e.g. wearables, mobile phones, implanted devices) and larger systems (cars, factory equipment, roads and bridges, supercomputers etc.) need to continuously scale with each successive generations. Moore’s law enables device scaling. Advanced interconnects and packaging technologies enable system-scaling. In this presentation, recent developments in interconnects and packaging technologies that will enable IoT will be presented. Some of these technologies include high density Fan-Out Wafer Level Packaging, passive and active Interposers, WLCSP for MEMS and Sensors.
About iNEMI

The International Electronics Manufacturing Initiative (iNEMI) is a not-for-profit, highly efficient R&D consortium of approximately 90 leading electronics manufacturers, suppliers, associations, government agencies and universities. iNEMI is based in Herndon, Virginia, with regional offices in Asia (Shanghai and Tokyo) and Europe (Limerick, Ireland). We are led by an international board of directors with management depth who represent a cross-section of the electronics manufacturing industry.

Forecast and accelerate improvements in the electronics manufacturing industry for a sustainable future. iNEMI roadmaps the future technology requirements of the global electronics industry, identifies and prioritizes technology and infrastructure gaps, and helps eliminate those gaps through timely, high-impact deployment projects. These projects support our members' businesses by accelerating deployment of new technologies, developing industry infrastructure, stimulating standards development, and disseminating efficient business practices. We also sponsor proactive forums on key industry issues and publish position papers to focus industry direction.

For additional information: http://www.inemi.org