Substrate Technology Discussions of 2.1/2.5D IC Packaging Process

K. Ano
Shinkawa Ltd.,
Kazuaki-ano@shinkawa.com
Outline

- Introduction of TCB packaging
- Substrate discussions for future needs
- Equipment functions for fine pitch TCB
- Summary
Introduction of TCB Packaging
Thermo Compression Bonding Process

(Apply NCP/NCF) → Chip P’n Place → Touch down

Heat up & Press → Cool down → Release & Take off

NCP/NCF need high force!
Motivation of C4/C2 → TCB

1. Bump pitch
2. Si die thickness
3. Process cost

Bump Pitch Roadmap Reference (R. Nair, Foundry perspective of 2.5D&3D integration, Semicon Singapore 2013)

Process transition by Bump pitch

Die thickness (um)

Process transition by Si die thickness
<table>
<thead>
<tr>
<th></th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Min. Inline pitch (um)</strong></td>
<td>50</td>
<td>30</td>
<td>30</td>
<td>25</td>
</tr>
<tr>
<td><strong>Min. Staggered pitch (um)</strong></td>
<td>40/80</td>
<td>30/60</td>
<td>30/60</td>
<td>30/60</td>
</tr>
<tr>
<td></td>
<td>(2 rows)</td>
<td>(3 rows)</td>
<td>(3 rows)</td>
<td>(3 rows)</td>
</tr>
<tr>
<td><strong>Max. Die Size (mm)</strong></td>
<td>12x12</td>
<td>19x19</td>
<td>28x28</td>
<td>28x28</td>
</tr>
</tbody>
</table>

*(Ref. AMKOR @SMTA Expo 2012.12)*

<table>
<thead>
<tr>
<th></th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bond accuracy (um)</strong></td>
<td>2.0</td>
<td>2.0</td>
<td>2.0</td>
<td>1.5</td>
</tr>
<tr>
<td><strong>Min. Die thickness (um)</strong></td>
<td>25</td>
<td>25</td>
<td>25</td>
<td>20</td>
</tr>
<tr>
<td><strong>Max. Bond Force (N)</strong></td>
<td>300</td>
<td>500</td>
<td>1000</td>
<td>??</td>
</tr>
</tbody>
</table>

*(Ref. Shinkawa challenge)*
Technical discussions for future needs

Substrate
- CTE and placement accuracy
- Land position accuracy
- Pillar size vs land size (length)
- Lead width and bonding force
- Fiducial accuracy for post bond inspection

Equipment
- Thin die handling
- Tool Parallelism
- Technical Challenges
Substrate discussions for future TCB Packaging
Pillar Pitch vs Placement Accuracy

Substrate & Packaging Technology Workshop 2014.4.22

Pillar pitch vs Bonding Accuracy Needed by Chip size (mm)

C2S: Epoxy-Glass base substrate

Small Die

Large Die

Temp. 80c → 240c
dT=160c
Si: 3ppm
Sub:13ppm

Placement Accuracy

Offset by Thermal expansion

W=0.4xPitch

Low CTE substrate is needed!
Substrate land position accuracy analysis

Offset
\[ X = \text{Lead Center } X - \text{Det. Pattern Center } X \]
\[ Y = \text{Lead Center } Y - \text{Det. Pattern Center } Y \]

\[ L = \text{Pattern distance} \]

- Measured @ room temp.
- 5 times repeat measurement per unit by vision system.
Unit center offset measurement results

Fiducial mark cannot be accurate position reference.

Small PKG

Large PKG
Limitation of TC-CUF(Capillary Under-Fill) process

Thermal shrinkage after soldering generate stress on pillar or solder joint. This is identical phenomena with BGA PKG’s solder pad design.

Needs pre under-fill material(NCP/NCF) for fine pitch soldering.
Future High Force concerns for fine pitch NCP/NCF process

By decreasing the pillar pitch, lead width becomes skinny. If Bond Stage rigidity is not enough to high force, Cu pillar shifts and drop from the lead finally. This will be a bond offset issue.
Post Bond Inspection Idea

- Post Bond Inspection is requested by several customers.
- Placement fiducial must be the origin of the actual bond position measurement.
- Needs accurate patterning for future use.
Equipment Functions for Fine Pitch TCB
What will be needed for fine pitch TCB?

1. Solder cap height will decrease less than 5um! → Si die parallelism becomes critical to keep consistent solder joint gap.

2. Die thickness becomes much thinner! → Fragile thinned die is very difficult to handle.