The Requirement of Future Substrate
- Maker Point of View -

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Agenda

- Introduction to Next Generation Packaging Requirements
- Organic Substrate Requirements
  - Process development
  - Line width
- New laminate substrate structure to meet future electronic packaging requirements
  - Package on Package (PoP) for mobile application
  - Embedded Interposer Carrier (EIC) for high density interconnection
- Conclusions
- Question and Answer
Mobile and Cloud Applications Drive the Package Development

- System packaging needs
  - Small form factor
  - High performance
  - High bandwidth
  - Low power consumption
  - Low cost
  - Environmental Friendly
Technology to Meet Substrate Requirements

- **Thin Profile:**
  - Thinner core, Thinner dielectrics
  - Thinner dielectric
  - Coreless
  - Layer reduction

- **High Performance**
  - Embedded passive
  - Embedded active, embedded...

- **Fine line and Via Technology**

- **Assembly Technology**
  - TCFC, Micro ball
  - PoP
IC Laminate Substrate Technology Development Trend

IC Substrate
- Materials
  - Core
  - Build up Film (ABF)
  - PP
- Fine Line and Via
  - 8/8, 5/5, 3/3, 2/2, 1/1 µm
  - 60, 50, 40, 30, 20 µm
  - ENEPIG, ENIG, EPIG
- Surface Finishing
  - OSP, IT
  - DSOP, SPOP
- Joining
  - BOL, TCFC
- Embedded
  - Passive
  - Active
- Interposer
  - Glass Interposer
  - Organic Interposer
Organic Substrate Materials

Core Materials

Dielectric Materials

- HVM
- LVM
- R & D

Company A
Company B
Company C
Company D

Young's modulus (GPa)

CTE (ppm/°C)

04/2014

Df

Dk

Company A
Company B
Company C
Company D
Company E
Fine Line Solutions

- **Target Line Width**
  - Copper trace, 10/10 um 2013, 8/8 2014, 5/5 2015, 3/3 2/2 2016, 1/1 2017
  - Target Via size, 60 um 2013, 50 um 2014, 40 um 2015, 30 um 2016
- Lines 8/8 um and possible 5/5 um lines can be achievable by current organic lamination process.
- But below 5/5 um, methods under consideration:
  - Semi additive
  - Line first by embedding
  - Line last by embedding
  - Copper Damascening
- **Photo Process**
  - Exposure tool, Stepper, LDI, but need large panel processing
  - Liquid photo resist may be required.
  - Slit coating, Spin coating of PR
- **Planarization**
  - Large Area CMP may be needed..
Substrate Structure - Unimicron Innovation and Solutions
New Advanced FCBGA Factory

- HVM lines for fine line (10/10 μm) & fine bump pitch (≤125μm)

Adv. Exposure system
u-ball FC line

Class 100 clean room facility
Lithographic Tool Status

Exposure Tool Capability

- A company LDI
- B company LDI
- B company Stepper
- C company Stepper
- D company Stepper
# Line Embedded Technology

<table>
<thead>
<tr>
<th></th>
<th>Line First PLP</th>
<th>Line Last PLP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper Line Formation</td>
<td>Copper line formed before dielectric</td>
<td>Copper line formed after dielectric</td>
</tr>
<tr>
<td>Cavity=line formation</td>
<td>SAP copper</td>
<td>Photo sensitive Dielectric, Laser trench</td>
</tr>
<tr>
<td>Structure Formation</td>
<td>Lamination</td>
<td>Copper plating + Planaration</td>
</tr>
<tr>
<td>Density capabilities</td>
<td>Down to 5 um, via 30 um</td>
<td>Down to 5 um, via 30 um</td>
</tr>
<tr>
<td>Cost down Potential</td>
<td>Better</td>
<td>Basic</td>
</tr>
</tbody>
</table>
Line Last Embedded Technology

- Laser or photosensitive dielectric trench formation
- L/S < 8/8 um fine pitch trench can be formed
- Better adhesion than SAP process
- Challenges:
  - Materials availability, need fine filler size dielectric or filler-less
  - Copper line revealing process
Line First Embedded Technology

- SAP copper trace formation
- L/S < 5/5 um can be formed
- Better copper trace adhesion than SAP process
- Challenges:
  - More than one LE layer
  - Packaging industry acceptance

<table>
<thead>
<tr>
<th>L/S</th>
<th>8/8um</th>
<th>7/7um</th>
<th>6/6um</th>
<th>5/5um</th>
</tr>
</thead>
<tbody>
<tr>
<td>3000×</td>
<td>![Image](543x35 to 578x755)</td>
<td>![Image](363x71 to 491x721)</td>
<td><img src="572x93" alt="Image" /></td>
<td><img src="115x157" alt="Image" /></td>
</tr>
</tbody>
</table>
Structure Roadmap of Memory AP Connections

PoP Package
(Die Last)

TMV PoP Package

HCP PoP Package
(over 1000 I/O)

FOWLP Package
(Die First)

Embedded Package

FOWLP PoP

## FO-WLP and PLP Process Comparison

<table>
<thead>
<tr>
<th></th>
<th>FO-WLP</th>
<th>PLP</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Structure</strong></td>
<td>![FO-WLP Diagram]</td>
<td>![PLP Diagram]</td>
</tr>
<tr>
<td><strong>Substrate Size</strong></td>
<td>Δ</td>
<td>O</td>
</tr>
<tr>
<td><strong>Symmetrical Build</strong></td>
<td>No</td>
<td>Yes*</td>
</tr>
<tr>
<td><strong>L/S-Routing Density</strong></td>
<td>O</td>
<td>Δ</td>
</tr>
<tr>
<td><strong>Thickness</strong></td>
<td>O</td>
<td>Δ</td>
</tr>
<tr>
<td><strong>Equipment Cost</strong></td>
<td>Δ</td>
<td>O</td>
</tr>
<tr>
<td><strong>3D Extendibility</strong></td>
<td>O</td>
<td>O</td>
</tr>
<tr>
<td><strong>Cost Down Potential</strong></td>
<td>Δ</td>
<td>O</td>
</tr>
</tbody>
</table>

*O: Good; Δ: OK

*: Single side possible
### WLP and PLP

<table>
<thead>
<tr>
<th></th>
<th>Wafer Level Package (WLP)</th>
<th>Panel Level Package (PLP)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Processing Size</strong></td>
<td>12”</td>
<td>20” or larger</td>
</tr>
<tr>
<td><strong>Material Base</strong></td>
<td>Major is silicon, but glass and organic are possible</td>
<td>Major in organic but glass or a-silicon are possible</td>
</tr>
<tr>
<td><strong>Equipment</strong></td>
<td>Semiconductor centric; Stepper, coater, sputter..</td>
<td>Organic substrate centric; Laser via, e-less, lamination of dielectric..</td>
</tr>
<tr>
<td><strong>Density Capabilities</strong></td>
<td>Down to 1 um L/S, via 5 um</td>
<td>Down to 5 um L/S, via 30 um</td>
</tr>
<tr>
<td><strong>Cost down Potential</strong></td>
<td>Baseline</td>
<td>Better</td>
</tr>
</tbody>
</table>
Memory Bandwidth Requirements in the Future

Mobile Device Evaluation Trend

2005
- LPDDR
  - 1.8V
  - ~400Mbps / pin
  - ~1.6GBps (x32)

2010
- LPDDR2
  - 1.2V
  - ~1066Mbps / pin
  - ~4.3GB/s (x32)
  - ~8.5GBps (x64)

2013
- LPDDR3
  - 1.2V
  - ~1866Mbps / pin
  - ~7.5GB/s (x32)
  - ~15GBps (x64)

2015
- LPDDR4
  - 1.1V
  - ~3200Mbps + / pin (ODT)
  - ~12.8GB/s (x32)
  - ~25.6GBps (x64)

Question mark

Under developing now

No market

Wide IO
- 1.2V
- 266Mbps/pin
- 17GB/s (x512)

Wide IO2
- 1.1V
- 800Mbps/pin
- 25.6GBps (x256)
- 51.2GBps (x512)

Source: SK hynix

Unimicron
# Evolution of POP Structure

<table>
<thead>
<tr>
<th>Generation</th>
<th>Technology</th>
<th>Pitch (mm)</th>
<th>Support I/O</th>
<th>Structure</th>
<th>Company</th>
</tr>
</thead>
<tbody>
<tr>
<td>G1</td>
<td>Solder Ball</td>
<td>0.5</td>
<td>~100</td>
<td><img src="image1.png" alt="Image" /></td>
<td>OSATs</td>
</tr>
<tr>
<td>G2</td>
<td>Through Mold Via</td>
<td>0.5 to 0.4</td>
<td>~300</td>
<td><img src="image2.png" alt="Image" /></td>
<td>Amkor</td>
</tr>
<tr>
<td>G3</td>
<td>Solder coated copper ball</td>
<td>0.5 to 0.3</td>
<td>~400</td>
<td><img src="image3.png" alt="Image" /></td>
<td>Shinko</td>
</tr>
<tr>
<td>G4</td>
<td>High Copper Pillar</td>
<td>0.5 to 0.1</td>
<td>Over 1000</td>
<td><img src="image4.png" alt="Image" /></td>
<td>Unimicron*</td>
</tr>
</tbody>
</table>

*: DC Hu, etc. ECTC 2013
High I/O Counts PoP Approaches

- HCP: High Cu Pillar (Unimicron)
- TMV: Through Mold Vias (Amkor)
- MCeP: Molded Core embedded Package (Shinko)
- BVA: Bond Via Array (Invensas)
- PIP: Package Interposer Package (Endicott Interconnect)
- CP: Copper Post (Amkor)
Interposer Value Proposition

- Reduce the cost of interposer by:
  - EIC structure
  - Large panel process
  - Lamination Dielectric
  - Laser via drilling
  - E’less copper
  - PCB Copper plating line

Line Width (um)

TPV Via Diameter (um)

IC Fab
Si Interposer
(Performance)

Unimicron FC-EIC
(Value)

PCB & Carrier
(Low Cost)
FC-EIC® Benefits

- FC-EIC® has **low profile** and **cost benefit** than ColoS.
  - This structure eliminates the solder joining between the interposer and the laminated organic substrate.
  - The connections of interposer to carrier in EIC structure are copper to copper which have less resistance and inductance compare to the conventional solder joints; **better electrical performance**.
  - Know good EIC substrate, reduce chip assemble loss.
  - Interposer is protected by the carrier in EIC structure.
    - Large interposer sizes are possible.
    - Thin interposers (30 or 50 um thickness) can be included in EIC structure. Thin interposers have a **lower processing cost** in via forming and via plating.
  - EIC structure has a **lower profile** than ColoS.
  - EIC structure is compatible with current backend infrastructure.
**Unimicron’s Solution - EIC Basic Structure**

- Combine interposer and organic substrate.
  - **Eliminates** the solder joints between interposer and organic substrate.
- Benefits:
  - Layer reduction compared with conventional organic substrate.
  - Alternative solution for high density SiP.
  - Cost reduction by interposer/carrier integration.

*DC Hu, TJ Tseng, YH Chen, WJ Lo* ECTC 2013
Chip on Interposer on Substrate vs. FC-EIC®

- **Chip on Interposer on Substrate: (ColoS)**
  - Interposer need double side RDL/Bumping and assembly process.
  - Four testing steps are used: Interposer, carrier, Interposer+carrier, chip+interposer +carrier.

- **FC-EIC®: Flip Chip – Embedded Interposer Carrier**
  - Interposer need to be embedded into the substrate.
  - Only two testing steps are used: interposer, and interposer+carrier.
  - Risk of thin wafer handling process is reduced.
EIC Application

Single Chip

[Diagram of a single chip setup]

Multiple Chips, SiP

High Density Memory
HMC, HBM, Wide I/O 2

[Diagram of multiple chips setup]
The Changing Role of Organic Substrate

New Role of Substrate in 3D ERA

- Panel Level Module Integration -

Now

Future

Optical Fiber
## Which Advance Packaging Technology may Win in Next Three Years?

<table>
<thead>
<tr>
<th>Technology</th>
<th>Technology Trend</th>
<th>Challenges</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Die First</strong> (include multiple dies)</td>
<td></td>
<td>Materials: Low CTE, Low Df</td>
</tr>
<tr>
<td>FO-WLP</td>
<td></td>
<td>Equipment: Die bonder Photo tool – LDI, Stepper</td>
</tr>
<tr>
<td>PLP Embedded Technology</td>
<td></td>
<td>Cost</td>
</tr>
<tr>
<td><strong>Die Last</strong> (include multiple dies)</td>
<td></td>
<td>Materials: Low CTE, High Tg, Low Df</td>
</tr>
<tr>
<td>Interposer (2.5D)</td>
<td></td>
<td>Equipment: LDI, Stepper</td>
</tr>
<tr>
<td>Silicon</td>
<td></td>
<td>Cost</td>
</tr>
<tr>
<td>Glass</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Organic</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FC-EIC</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: *Target supporting 2 um lines* except PLP Embedding Technology.
Summary and Conclusions

1. Due to the advance of mobile and cloud, substrate underneath the chip is undergo evolution and revolutionary changes.

2. Substrate core materials are fine tuning to low CTE with high modules. And dielectric materials with better surface quality and low dielectric loss is in demand.

3. Due to the fine feature requirements in the substrate, some process module may in the transition of from pure wet process to dry process. The equipment from semiconductor and flat panel display industry are finding place in substrate companies.

4. Substrate structure is not the simple copper trace laminated by organic dielectric materials. Substrate can embedded passive components, active components, interposers or even optical fiber in the future. Substrate can act as system integrator of electronic components in 3D structure.

5. Die first and Die last solutions will give customers more freedom in packaging selection.
Thank You!

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