Challenges to Consider in Organic Interposer HVM

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Outline

• Today’s organic interposers for FC-BGA substrates (here is what we can produce)
• Today’s 2.5D silicon interposers
• Plans for glass interposers
• Potential for organic interposers
• Issues for organic interposers
Trends in FC-BGAs

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>2013</th>
<th>2015</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ball Count Range</td>
<td>400 to 3,000+</td>
<td>400 to 4,000</td>
</tr>
<tr>
<td>Body Size Range (mm)</td>
<td>21 x 21 to 65 x 65</td>
<td>17 x 17 to 72 x 72</td>
</tr>
<tr>
<td>Typical Construction</td>
<td>Build-up, up to 8-2-8 layers</td>
<td>8-2-8</td>
</tr>
<tr>
<td>Line/Space (µm)</td>
<td>Min. 9/12 on build-up layers</td>
<td>≤8/8</td>
</tr>
<tr>
<td>Via/Pad Diameter (µm)</td>
<td>≤60/90 on build-up layers</td>
<td>&lt;45/80</td>
</tr>
</tbody>
</table>

Source: TechSearch International, Inc.

- Warpage remains a challenge
- Increased interconnect density drives finer feature sizes
- Increased implementation of coreless substrates for future designs
- Continued use of surface mount capacitors for high-performance (FC-CSP uses embedded capacitors)
Today’s Silicon Interposers

• Advantages
  – Partitioning large die
  – Planar module with stacked memory adjacent to the processor for high speed memory requirements, can be tested prior to assembly
  – Manage chip/package interaction stress for large die with ultra low-k dielectrics
  – Reduce die size where substrate density is the constraint
  – Can incorporate integrated passives
  – An interim solution before 3D IC with TSV is possible
Xilinx “Stacked Silicon Interconnect” (2.5D)

- Xilinx 28nm Virtex-7 LX2000T is a 2.5D FPGA solution using a silicon interposer
  - Four FPGA “slices” are co-designed on a 28nm silicon node technology
  - FPGA slices sit side-by-side connected using Amkor’s Cu pillar micro bumps to a passive silicon interposer fabricated with 65nm silicon node technology
  - Silicon interposer contains TSVs with aspect ratio of 10:1
  - Silicon interposer is connected to organic build-up substrate using C4 bumps

- Improved performance
- Lower power
- Xilinx announcement will drive the capacity for silicon interposers, just as it did for 300mm bumping

Source: Xilinx
High-Performance Interposer Market

• FPGA
  – Four products shipping today from Xilinx, various sizes of interposers
  – Homogeneous integration solution is partition die so that the large die can be fabricated in “slices” providing better yield, improved performance
  – Heterogeneous solutions includes FPGA slices and transceiver die
  – Small volume, but helps to develop infrastructure

• GPU/CPU
  – Provide higher performance with memory stack next to processor

• ASIC
  – High-end applications where ASIC is mounted on an interposer next to a memory stack
  – An interposer to mount the silicon with ELK dielectric before mounting on package substrate
Silicon Interposer Suppliers

- Foundry Interposers with TSVs
  - ALLVIA
  - TSMC
  - UMC
  - IBM
  - GLOBALFOUNDRIES
  - Novati Technologies
- OSAT Interposers with TSVs
  - ASE
  - SPIL
  - PTI
- Interposers for MEMS with TSVs
  - DNP
  - IMT
  - Silex Microsystems
  - Others
- Interposers with Integrated Passives (with or without TSVs)
  - IPDiA
  - STATS ChipPAC
Barriers to Silicon Interposer Implementation

• Infrastructure immaturity
  – All components of technology are not ready for immediate implementation, especially for fabless companies
  – Supply chain handoff needs to be defined
  – Assembly by OSAT or Foundry?
  – Is there test or only inspection? Who is in charge?

• Cost
  – Especially for high via counts
  – Yield hit for large substrates
  – Biggest cost driver is yield loss, not process cost (SavanSys Solutions)
  – Glass interposers for lower cost?
  – Organic interposers as an alternative?

• Reticle Field Size
  – Maximum front-end reticle field size = 26mm x 32mm
  – Back-end steppers have larger exposure fields, coarser traces
Organic Interposers

- Under consideration as lower cost alternative to silicon interposers
  - Infrastructure established
  - Examples of organic substrates in production for multi-chip modules

- Today’s feature sizes for organic substrates from major suppliers with build-up process
  - Minimum bump pitch supported ranges from 120 to 150 µm
  - Minimum line widths and space 9/12 to 14/14 µm
  - Minimum via/pad 30/60 to 60/100 µm

- Coreless substrate technology has been introduced
Advantages of Organic Interposers

- Definition differences (no consensus in industry)
  - 2.5D: Silicon-like structure with fine features, small vias (many R&D activities)
  - 2.1D: One or two layers of fine line on conventional organic substrate (increasing number of solutions)
- Potential applications by 2015
- Potentially lower cost than silicon
- Simpler manufacturing process flow
- Today’s features range from 2µm line/space to 10µm line/space
- Existing infrastructure for manufacturer and assembly, suppliers with R&D include:
  - Ibiden
  - Kinsus
  - Kyocera SLC
  - NTK
  - Samsung Electro-Mechanics
  - Shinko Electric
  - Unimicron
## Organic Interposers

<table>
<thead>
<tr>
<th></th>
<th>Organic Interposer</th>
<th>Silicon Interposer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Core Substrate Type</strong></td>
<td>Panel</td>
<td>Wafer</td>
</tr>
<tr>
<td><strong>Core Material, CTE</strong></td>
<td>Organic, 4ppm/K</td>
<td>Silicon, 3ppm/K</td>
</tr>
<tr>
<td><strong>Core Thickness</strong></td>
<td>60 - 450µm</td>
<td>100µm</td>
</tr>
<tr>
<td><strong>Structure, Top + Bottom</strong></td>
<td>Symmetry (n+n)</td>
<td>Asymmetry (n+1)</td>
</tr>
<tr>
<td><strong>Core Through-Hole</strong></td>
<td>Laser Via / Mechanical Drill</td>
<td>Dry Etch</td>
</tr>
<tr>
<td><strong>Thickness Control</strong></td>
<td>Core Thickness Selected</td>
<td>Wafer Thinning</td>
</tr>
<tr>
<td><strong>Linewidth</strong></td>
<td>3µm in 2013</td>
<td>1µm</td>
</tr>
<tr>
<td><strong>Net Die (25mm x 25mm)</strong></td>
<td>1,260 units/m² (200mm x 250mm panel)</td>
<td>801 units/m² (300 mm wafer)</td>
</tr>
</tbody>
</table>

Source: SEMCO

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iNEMI Substrate & Packaging Workshop, Toyama, Japan 21st April 2014
Challenges for Organic Interposers

• Inherently lower density than silicon
• Meeting required density while maintaining reliability and cost
• New dielectric materials may be required to handle warpage, fine features, and provide low CTE for microvia reliability
• Surface roughness of the organic substrate
• Trace cracking a very fine line widths (2 µm)
• Metallization/adhesion for via integrity and fine patterning
  – Thin seed layer (minimizing metal etch) for fine (3µm L/S)
  – Adhesion promotion for seed layer
  – Non-contact methods of patterning for high resolutions to minimize contamination
  – Clean process that provides high etch uniformity
Challenges for Organic Interposers

- < 5µm L/S fabrication methods may include
  - Semi-additive process
  - Line first or line last by embedded
  - Copper damascene process (expensive)

- Photo process for fine features may require
  - Exposure tool such as stepper or laser direct imaging (need large panel process)

- Planarization
  - Large area CMP may be needed

- Inspection?
  - Current AOI methods can’t resolve core fine features or debris in vias
  - In process inspection may be required to improve yield (to lower cost)
New AOI Tools Needed for Fine Features

White Light Image
Copper on FR4

0.7 Micron Pixel

Fluorescent Image
Copper on FR4

Defects

4 µ nick

6 µ open

2 µ short

Source: Beltronics

iNEMI Substrate & Packaging Workshop,
Toyama, Japan 21st April 2014
New AOI Needed to Find Debris in Vias

White Light Image 1.75 µ Pixel Fluorescent Image

Source: Beltronics
Glass Interposers

• Advantages
  – Formed by fusion, does not require thinning or polishing
  – Flat surface
  – Specialty elements can be added to control thermal and electrical properties
  – Typical Young’s modulus 40 to 120 GPa, CTE 3 to 12 ppm/°C

• Challenges
  – Warpage control for large panels
  – Backend processing such as sawing and back-grinding are concerns
  – Cost effective via formation and metallization for thousands of small vias, potentially narrow process window
  – Fracture toughness of glass low
  – Stress corrosion cracking could occur
  – Concerns with high-frequency applications
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Potential Glass Interposer Suppliers

- **Asahi Glass:** “E-Discharging” process uses a laser to heat the local area resulting in a smooth via with a clean entrance
  - Typical vias have 60µm entrance and 40µm exit diameters
  - Maskless process
  - Throughput of 1,000 vias per second reported
  - Typical panel size 450 mm x 500 mm
  - Process in roll-to-roll or panel format
  - Work underway to metallize 50µm via on 130µm pitch
  - Signed agreement with U.S. start-up nMode to create Triton Micro Technologies for development of novel filling technology using thin glass

- **Corning:** Focused on alumina silicon glass “Willow” for interposers
  - Can be tailored in range of 3.2 to 9 ppm/°C
  - Typical vias 30 to 50µm diameters on 100µm pitch
  - Small vias with 20µm diameters have been fabricated
  - Working on fusion roll-to-roll process
  - Research with Georgia Tech and ITRI
GA Tech Demonstrations of Glass Interposer with TPV

- Ultimate potential of glass
  - 30µm thickness
  - 5µm TPV diameter
  - 20µm pitch
  - 700mm size
  - Resistivity same as SiO₂
  - Loss same as SiO₂
  - TCE Optimized for Si & PWB

Source: Georgia Institute of Technology
Conclusions

- Many options to consider for interposers (each has + and -)
  - Silicon interposer (today’s solution)
  - Organic interposer (a possibility)
  - Glass interposer (a future solution?)
- 2.5D Applications: The New MCM
  - Same challenges as in the past
- Infrastructure and Cost key to successful adoption
Thank you for your kind attention!

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