Key Technology Challenges in Computing Package and Assembly

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Agenda

- **Key Messages**
- **Technology Drivers**
  - The Evolving World of Computing & Data
- **Industry Challenges**
  - First Level & Second Level Interconnect Pitch Scaling
  - 2.5D & 3D Packaging
  - Ultra Thin Packaging
  - IoT & Wearable Packaging
- **Closing Remarks**

*IoT: Internet of Things*
Key Messages

• Technology getting more complex Gen-over-Gen….
  – Moore's Law is alive and fueling the “Compute Continuum” revolution
  – Packaging is a key enabler of the Si scaling & Computing User experience

• Significant Opportunities Enabled by Next Generation Packaging
  – Industry wide investment and innovations required
  – Require total Assembly solution
    – Equipment, process, Material & Total Cost of Ownership
  – Need Direct Collaboration across the supply chain
Agenda

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- Closing Remarks
Executing to Moore’s Law
A Predictable Silicon Track Record

Enabling new devices with higher functionality and complexity while controlling power, cost, and size

90 nm
65 nm
45 nm
32 nm
22 nm
14 nm
10 nm
7 nm

Hi-K Metal Gate
3D Transistors

Strained Silicon
Packaging Evolves As Scaling Creates New Markets

1970's
A) Wirebond  
B) Leadframe  
C) Plastic & Ceramic  
D) Low Pincount DIPs

1990's
A) Wirebond & Flipchip  
B) Laminate  
C) Ceramic & Organic  
D) High Pincount PGA  
Thermally Enhanced

2010's
A) Pb-Free Flipchip  
B) Very Thin Laminate  
C) Organic  
D) High Pincount LGA & BGA  
Ultra-Small Form Factors
Conflict-Free Processors

Au 79
Gold

Ta 73
Tantalum

Sn 50
Tin

W 74
Tungsten

INEMI Substrate & Package Technology Workshop 2014

Kinya Ichikawa
A New World of Personalized Computing
Cost Effective Processing Available Everywhere

2020: 31 Billion Connected Devices & 4 Billion Connected People
Source: IDC
Incredible Growth in Data Consumption
Growth in mobile devices is having a tremendous impact on data traffic

What Happens in an Internet Minute?

And Future Growth is Staggering

Today, the number of networked devices = the global population
By 2015, the number of networked devices = 2x the global population
In 2015, it would take you 5 years to view all video crossing IP networks each second
Industry Trends in Computing Packages
Expanding Portfolio of Solutions

- Wearables/IoT
- Ultra-Mobile
- Client
- Data Center

<table>
<thead>
<tr>
<th>I/O Count</th>
<th>Chip to Package Area Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>1</td>
</tr>
<tr>
<td>500</td>
<td>2</td>
</tr>
<tr>
<td>5000</td>
<td>5</td>
</tr>
</tbody>
</table>

- WLP/DCA
- FC-CSP
- PoP
- FC-BGA
- FC-LGA

- Pitch Scaling
- 2.5D/3D integration
- Ultra-thin and small
- Low Cost WLP/DCA

IoT: Internet of Things
Technology Driver & Challenges

1. The first level interconnect (chip to package) and the second level interconnect (package to board) **Pitch Scaling** are the essential to decrease the gap with the relentless silicon technology scaling.

2. Increasing bandwidth density within the package drives innovation including logic and memory interconnects with **2.5D and 3D Integration**.

3. Meeting the push for **Ultra-Thin** form factors will require advances in thin wafer handling, thin die assembly, thin substrate manufacturing, and package warpage controls.

4. System densification in Wearable/IoT drives innovations in **Wafer Level Packaging / Direct Chip Attach and Low Cost Flip Chip technology** to enable further reduction in cost, size and power.
Agenda

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Technology Driver & Challenges

Driver #1

The first level interconnect (chip to package) and the second level interconnect (package to board) **pitch scaling** are the essential to decrease the gap with the relentless silicon technology scaling.
Chip-to-Package Interconnect
Trend in Minimum Flip Chip Bump Pitch at Intel

Bump pitch scaling challenges include chip attach, Chip-Package-Interaction & substrate advancement.
Key Industry Challenges for FLI Scaling
Creating a Robust Flip Chip Interconnect

- Chip-Package-Interaction
  - Low K ILD Integration
- Assembly Process Yields
  - Solder collapse vs. Warpage
- Joint Fatigue
- Current Carrying Capability

- Flip chip Metallurgy
  - Cu bump with Pf free solder, Cu-Cu
- Chip Attach Process
  - Reflow, TCB and die embedded
- Underfill
  - Capillary, Mold and Pre-applied

Chip-Package-Interaction
Assembly Yield
Bump Crack
Electro Migration
Solder Collapse Chip Attach Fine Pitch & Smaller Solder Bumps Limited by Die & Substrate Dynamic Warpage

Mass Reflow Flip Chip

TCB Flip Chip

Thermal Compression Bonding Process for Fine Pitch Chip Joint (less than 100um pitch)

- X/Y & Z Placement Accuracy
- Precision temp control
- Process Cost
- Require Integration of Fluxing and Underfill

Die warpage = function of die diagonal length and thickness
Substrate and Board Technologies Scaling
Required to take full advantage of Si-scaling

Advanced, alternate technologies to achieve a low cost solution to enabling finer L/S (<10 μm) pitch

Alternate technology needed to shrink via size and tolerance
Low CTE materials needed for improved via reliability
Second Level Interconnect Challenges
Overcoming Warpage to Solder the SOC Package to the PCB

Key Challenge: Managing Package Warpage to Enable Fine Pitch BGA Surface Mount
<table>
<thead>
<tr>
<th>Technology</th>
<th>FLI Pitch</th>
<th>Technical Challenges</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mass Reflow</td>
<td>&gt;100um</td>
<td>• X/Y Placement Accuracy</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Solder Collapse vs Warpage Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Managing Post Reflow Mechanical Stress on Package or on PCB</td>
</tr>
<tr>
<td>Thermo-compression Bonding</td>
<td>&gt;10um</td>
<td>• X/Y &amp; Z Placement Accuracy</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Precision Temperature Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Process Cost</td>
</tr>
<tr>
<td>Embedded Die</td>
<td>&gt;10um</td>
<td>• Materials Mismatch in Planar Structure</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Yield</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• TPT</td>
</tr>
<tr>
<td>Cu to Cu</td>
<td>&gt;1um</td>
<td>• X/Y Alignment</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Planarity</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Bond Time</td>
</tr>
</tbody>
</table>
## FLI Scaling
Flip Chip Interconnect Scaling Industry Challenges

<table>
<thead>
<tr>
<th>Technology</th>
<th>FLI Pitch</th>
<th>Application</th>
<th>Technical Challenges</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capillary Underfill</td>
<td>&gt;100um</td>
<td>Large die FCBGA</td>
<td>• Flow voids&lt;br&gt;• Large die / Narrow stand off&lt;br&gt;• Material and process optimization</td>
</tr>
<tr>
<td>Mold Underfill</td>
<td>&gt;100um</td>
<td>Low cost Strip Assembly</td>
<td>• Thin mold cap / die exposed mold&lt;br&gt;• Flow voids&lt;br&gt;• Mold design&lt;br&gt;• Material and process optimization</td>
</tr>
<tr>
<td>Pre-apply Underfill</td>
<td>&gt;40um</td>
<td>3D Memory Integration</td>
<td>• Implement with Thermo-compression bonding&lt;br&gt;• Filler entrapment / Reliability&lt;br&gt;• TPT</td>
</tr>
<tr>
<td>Wafer level Underfill</td>
<td></td>
<td>Still in research</td>
<td></td>
</tr>
</tbody>
</table>
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  - The Evolving World of Computing & Data

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- **Closing Remarks**
Technology Driver & Challenges

Driver 2

Increasing bandwidth density within the package drives innovation including logic and memory interconnects with **2.5D and 3D integration**

**2.5D Silicon Interposer with TSV**

Source: Intel Technology Journal 2007

Tera-scale computing

**Industry Challenge:**
Meet Product performance targets with affordable costs
Demanding Increasing CPU to Memory Bandwidth

Compute density becoming key in Phones/Tablets/IDC servers/Supercomputing
SOC Memory Bandwidth Requirements
A Key Element of Device Performance

Apple Memory Bandwidth Increasing with Generation to Improve Performance
Source: http://www.anandtech.com/

Memory Technology Continues to Evolve to Support SOC Requirements
Source: Samsung

New Packaging Architectures Are Required To Take Full Advantage Of Increasing Memory Bandwidth In Handheld Devices
# Mobile and High Performance Wide IO Applications

## 3D Stacked Package Drivers
- **High Band-width**: data transfer between chips
- **High Density**: Transistor & Interconnect
- **Low-Power**: smaller/no buffer, slow & wide interconnect
- **Small Form-factor**

### Computing Wide IO (High Performance) vs. Mobile Wide IO

<table>
<thead>
<tr>
<th>Structure Limitation</th>
<th>Thermal</th>
<th>Mobile Wide IO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cost</td>
<td>Dependent on design, technology and cooling technique</td>
<td>Serious</td>
</tr>
<tr>
<td>Data Band Width (Speed)</td>
<td>≤ 64 GB/s</td>
<td>≤12.8 GB/s</td>
</tr>
<tr>
<td>Power</td>
<td>10-150W</td>
<td>2-20W</td>
</tr>
<tr>
<td>Interposer</td>
<td>Can be used</td>
<td>Not Used</td>
</tr>
<tr>
<td>Structure for Thermal</td>
<td>Use heat sink and TIM</td>
<td>-</td>
</tr>
</tbody>
</table>

Source: JEDEC Server Memory Forum 2011

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**Diagram:**
- **Logic**
- **SLTV Interposer**
- **Heat Sink and TIM**
2.5 D interposer Solutions
Bandwidth Requirements Create New Challenges

2.5D Si Interposer
2.5D Glass Interposer
2.3 D Adv Org Interposer
2.3 D Adv Org Pkg

2.5D Interposer
• WI/O 2: 40um pitch
• HBM: 55um pitch
• L/S: 2um

Industry Cost Target
1.0 cent/mm² >
Source: Qualcomm

Source: Amkor
Source: JEDEC
## 2.5D Interposer Industry Challenges

<table>
<thead>
<tr>
<th>Technology</th>
<th>Design Rule (L/S &amp; Via Diameter)</th>
<th>Technical Challenges</th>
</tr>
</thead>
</table>
| Si interposer      | L/S 2um > via 10um >            | - Cost for large interposer  
                      |                                  | - Power delivery through TSV     |
| Glass interposer   | L/S 10um via 30um               | - Under development  
                      |                                  | - Looser design rule ?          |
|                    |                                  | - Low cost via drilling/ filling                                                    |
| Organic Interposer | L/S 2um – 5 um via 10 um-18 um  | - Under development  
                      |                                  | - Low cost process and materials  |
|                    |                                  |  (Dry vs. Wet process fungibility)                                                |
|                    |                                  | - Looser design rule / increased layers                                            |
|                    |                                  | - Low CTE core and co-planarity                                                    |
|                    |                                  | - micro via reliability                                                           |

Si interposer 30um via / 90um pitch
Glass interposer

Source: ITRI

Organic Interposer
Source: SEMCO 2012 MEPTEC

Si interposer
Source: SEMCO
Mobile Wide I/O DRAM 3D Assembly Challenges

- Chip Attach
- Chip placement accuracy and Low-force capability
- Material Dispense Integration
- Equipment Throughput

- Significant Opportunities Driven by 3D Stack Packaging
- Investment and innovations required
- Require turn key solution: Equipment, process & Material
- Need Direct Collaboration with Materials Suppliers
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Technology Driver & Challenges

Driver 3

Meeting the push for **ultra-thin** form factors will require advances in thin wafer handling, thin die assembly, thin substrate manufacturing, and package warpage controls.
Thin Is In!
Packaging Must Support Consumer’s Preference For Thinner, Sleeeker Devices

Thin Packaging Generates A New Set Of Thermo-mechanical Challenges Compared To Traditional PC Components!

Cross-section of iPhone 5
Package (SOC with Stacked Memory) is a significant contributor to overall phone thickness
SOC Packaging
Supporting Thinner and Smaller Devices

Key Challenge: Solving the Thermo-mechanical Issues That Arise As Packages Become Thinner And Interconnect Pitches Scale
The range of warpage on the interposer surface is very narrow.

*Interposer top surface remains flat through reflow, allowing the memory package to properly attach.*
Industry Mobile Computing Package

Through mold via shape

Source: Amkor 2008 ECTC

Warpage profiles over the reflow profile

TMV base PoP has become the de-facto package at OSAT for application processors

Mold material (thermo-mechanical/ shrinkage) properties are the key to manage warpage
Solution Space for Warpage Control

Warpage Solution Space consists of Geometry, Materials and Process

**Geometry**
- Package Dimensions
- Die/substrate/mold thickness
- BGA Size and Depopulation

**Materials**
- Low Temperature Solder
- Low Tg Underfill
- Low CTE & High Modulus Substrate
- Improved Board Paste

**Process**
- Molding (High modules and shrinkage)
- Stencil Optimization
- Variable SRO

Key Challenge: Research Needs to Focus on New Materials which Provide Warpage Control to Enable Thinner Packaging
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Driver 4

System densification in Wearable/IoT drives innovations in **Wafer Level Packaging / Direct Chip Attach and Low Cost Flip Chip technology** to enable further reduction in cost, size and power.
Flip Chip on HDI PCB

Typical Fine Pitch BGA

Mobile Products

APPLE iPhone 5 PCB
HDI PCB enable 0.4 mm pitch / 1326 balls CPU

Flip Chip Substrate to WLP Compatibility

Strong Smartphones, tablets demand drives the growth of the HDI / Type 4 PCB market

Future High End PCB's will support pitches that enable Logic Direct Chip Attach

Source: Prismark

Ten-Layer Construction
• 720μm thick
• 50μm L/S
• 50μm diameter
• 23 – 25μm copper thickness
• 35 – 50μm dielectric thickness

Source: Intel

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WLP to address future DCA needs

- Die Back side coat
- Si Chip
- Die Edge coat
- Die front side coat
- Solder bump

Source: Intel 2012 ICEP

Enables thinner system and lower package cost
Enables robust board assembly with advanced semiconductor generation
Low Cost Flip Chip Package

Industry has developed single-layer or two-layer low cost substrate technologies that simplify the substrate fabrication process as a way to provide a cost-effective advantage compared with existing solutions.
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Closing Remarks

- Growing portfolio of packaging solutions driven by new device use models and need for higher performance & form factor
- Significant Opportunities Driven by Next Generation Packaging
- Need increased level of investment & collaboration across the supply chain on developing total assembly solutions to overcome challenges associated with Pitch Scaling, 2.5D/3D integration, ultra-thin and Low Cost Packaging
Collaborative Development Example
- Virtual Pathfinding Line with Partners -

- Intel Lab: Quick turn analysis and feedbacks -

- External Labs: Virtual Full Process Capability -

• Able to run some early units for the early leanings
• Development work before the system is available