3D Packaging Solutions with Flip Chip and Fan-out Wafer Level Technology Driving Performance and Cost Innovation
Outline

1. STATS ChipPAC overview
2. Low cost flip chip solutions
3. Flip chip package on package (fc-PoP) experiences
4. Fan-out wafer-level package on package (eWLB-PoP) experiences
5. Summary
1. STATS ChipPAC overview
STATS ChipPAC At A Glance

- Tier-1 OSAT with broad manufacturing footprint
- Leader in turnkey solutions providing broad portfolio of packaging and test services
- Aligned with industry leaders in the communications, consumer and PC markets
- Innovator in advanced technology with key industry partnerships
- Patent portfolio ranked among the top 20 semiconductor manufacturing companies by IEEE for the last 3 years

Source: Company data.
Headquartered in Singapore, STATS ChipPAC has design, research and development, manufacturing and customer support offices strategically located throughout Asia, the United States and Europe.

**Shanghai, China (SCC)**
983K ft² facility provides wafer probe, assembly, test, memory card assembly and distribution services.

**Ichon, Korea (SCK and SCK2)**
770K ft² high-end facility specializes in advanced array packages such as Flip Chip, Stacked Die, CSP and BGA. Second 181K ft² facility focuses on wafer sort, probe, packaging and final test. New 1 million ft² facility expansion and consolidation to be completed by end of 2014.

**Yishun, Singapore (SCS)**
808K ft² facility with class 10K clean room. Provides wafer sort and bump, wafer level technology, fabrication of integrated passive devices, packaging and test services.

**Woodlands, Singapore (SCH-WD)**
51K ft² R&D facility specializes in next generation wafer level technologies such as Embedded Wafer Level BGA (eWLB) technology and Through Silicon Via (TSV).

**Hsin-Chu Hsien, Taiwan (SCT & SCT3)**
218K ft² test facility provides wafer probe and final test services, and flip chip R&D. Includes Class 100 cleanroom space for 300mm bump.

(1) IT Support Services
What We Do - Total Turnkey Solutions

Silicon wafers from foundry

Supporting customers in the mobile, cloud computing and wearable devices market segments

Outsourced Semiconductor Assembly and Test Services (OSAT)

- RDL/IPD
- Bump
- Probe
- Assembly
- Final Test
- Drop Ship

Customized solutions for multiple products / applications

- Fan-out wafer level packages
- Fan-in wafer level packages
- Flip chip packages
- 3D/stacked die & packages
- System-in-Package
- Laminate
- Leadframe
- Memory cards
# Manufacturing Sites Capabilities Overview

<table>
<thead>
<tr>
<th>Location</th>
<th>SCS - Singapore</th>
<th>SCK - Korea</th>
<th>SCC - China</th>
<th>SCT - Taiwan</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size (ft(^2))</td>
<td>808K</td>
<td>770K + 181K</td>
<td>983K</td>
<td>218K</td>
</tr>
<tr>
<td><strong>2014</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Assembly</strong></td>
<td></td>
<td></td>
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</tr>
<tr>
<td><strong>Portfolio</strong></td>
<td>200mm (Printed Bump), IPD, 8&quot; WLCSP, FBGA, QFN (punch, dual row) QFN-st, eWLCSP, eWLB, TSV</td>
<td>FBGA, FBGA-SD, PBGA, PBGA-H, PiP, PoP, SiP, FC-xBGA, FC-FBGA, FC-SiP</td>
<td>TSOP, TSOP-SD, FBGA-SD, FBGA, PBGA, PBGA-H, SiP, uSD, QFP, QFN, FC-xBGA, FC-FBGA, PoP, 200mm Plated Bump</td>
<td>300mm Plated Bump, WLCSP</td>
</tr>
<tr>
<td><strong>Test Focus</strong></td>
<td>Wafer Sort &amp; Final Test (RF, MS, Logic)</td>
<td>Wafer Sort &amp; Final Test (RF, MS, Memory Flash/SRAM/DRAM, Logic)</td>
<td>Wafer Sort &amp; Final Test (RF, MS, Analog, Logic, RFPA, Memory-Flash/SRAM/EEPROM)</td>
<td>Wafer Sort &amp; Final Test (Mixed Signal, Logic)</td>
</tr>
</tbody>
</table>
Our Strategy

Focus

Focus on Mobile Convergence
- Computing
- Communication
- Consumer

Align with Market Leaders
- Pick right customers and right programs (tiering & choice)

Differentiate

Technology Leadership: Differentiation thru Integration
- fcCuBE
- eWLBE
- TSV

Operation Excellence & Cost Competitiveness
- Consistent operational performance & continuing cost improvement

Test as Part of Turnkey
- Test as part of turnkey solution to win targeted programs + selected test only business

Computing Consumer

Operation Excellence & Cost Competitiveness

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Test as part of turnkey solution to win targeted programs + selected test only business

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STATSChipPAC®

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STATSChipPAC®
2. Low cost flip chip solutions
Flip Chip as Mainstream Technology
Flip Chip Cost Drivers by Market

### Computing/ Wired Communications
- OSAT flip chip ~ 300 Mu/year
- 8-14L substrate
- Large die/body size
- Thermal solution
- >0.7 mm pitch

### Consumer
- OSAT flip chip > 500Mu/year
- 4-6L substrate
- Medium die/body size
- May need thermal solution
- 0.4 - 1.0 mm pitch

### Mobile
- OSAT flip chip > 2Bu/year
- 2-4L Substrate
- Small die/body size
- Overmold
- 0.4 - 0.5 mm pitch
# Flip Chip Performance & Cost Drivers

<table>
<thead>
<tr>
<th>Cost Element</th>
<th>Performance Drivers</th>
<th>Cost Innovation</th>
</tr>
</thead>
</table>
| **Design**   | I/O Density, Performance - Substrate layers/Specs, Thermals Underfill - Pkg. Size | • fcCuBE  
• Mold Underfill (MUF)  
• Exposed Die |
| **Process**  | Si Reliability(ELK) - PI RPV  
Bump Reliability - Underfill  
I/O density - Mass Reflow/TCB | • fcCuBE  
• Mold Underfill (MUF) |
| **Materials**| Bump Reliability - Substrate materials, SOP, Core etc., Underfill | • fcCuBE  
• Mold Underfill (MUF) |

**fcCuBE Technology** drives overall cost improvement while meeting performance requirements
fcCuBE - Mass Reflow Extension

- 110 um / 55um Effective BP
- 49um UBM
- fcVFBGA MUF
- Qualified 28N
- HVM as of Q2 ‘13

100 um / 50um Effective BP
- 49um UBM
- fcVFBGA MUF
- 28N
- In Development
- HVM Q3 ‘14

80um / 40um Effective BP
- 40um UBM
- fcVFBGA MUF
- 20N
- ETS (Embedded Trace Substrate)
- Development as of Q4 ‘13
fcCuBE - Reliable Interconnect Technology

45N ELK → Passed All Reliability Testing
- 13.4x13.4mm pkg / 9.5x6.3mm die, 150u BP
- 4L(1-2-1), 0.24mm T substrate
- Reliability: MSL2AA, MSL3, TC’B’(2000cyc), HTST(1000hrs), uHAST(192hrs)

28N ELK → Passed All Reliability Testing
- 14x14mm pkg / 10.1x10.5mm die, 140u BP
- 4L(1-2-1), 0.24mm T substrate
- Reliability: MSL2AA, MSL3, TC’B’(2000cyc), HTST(1000hrs), uHAST(192hrs)
- Hammer Test (pre-underfill, multiple reflow test) passed 20X with no failure!

28nm Flip Chip

<table>
<thead>
<tr>
<th>Reliability Test</th>
<th>Pre-con</th>
<th>uHAST</th>
<th>TC&quot;B&quot;</th>
<th>HTST (w/o precon)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>96hrs</td>
<td>168hrs</td>
<td>200x</td>
<td>500x</td>
</tr>
<tr>
<td>O/308 (No Fail)</td>
<td>O/77 (No Fail)</td>
<td>O/77 (No Fail)</td>
<td>O/251 (No Fail)</td>
<td>O/251 (No Fail)</td>
</tr>
</tbody>
</table>
# Low Cost Substrate Technology

<table>
<thead>
<tr>
<th></th>
<th>STD</th>
<th>VUT</th>
<th>ETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>X-section View</td>
<td>![Image]</td>
<td>![Image]</td>
<td>![Image]</td>
</tr>
<tr>
<td>Cost 2L</td>
<td>100%</td>
<td>85 ~ 90% ↓</td>
<td>85 ~ 90% ↓ ↓</td>
</tr>
<tr>
<td>Cost 4L</td>
<td>100%</td>
<td>~40% ↓ ↓ (4L to 2L)</td>
<td>80%~85% ↓ ↓ (4L to 3L)</td>
</tr>
<tr>
<td>Patterning Process</td>
<td>SAP w/ PCF</td>
<td>MSAP</td>
<td>MSAP</td>
</tr>
<tr>
<td>Min Line/Space</td>
<td>15/15um SAP</td>
<td>15/15um SAP</td>
<td>8/10um MSAP</td>
</tr>
</tbody>
</table>
| Drivers        | Reference | • Cost reduction by design rule relaxation  
• Bump on Via  
• STD SOP, or;  
• BOL  
• Cost reduction by PCF Elimination  
• Lower Thickness  
• Fine Bump Pitch  
• Fine L/S  
• Enhanced MUF / CUF Process window |
3. Flip chip package on package (fc-PoP) experiences
fc-PoP Package Roadmap

Max Stack Height (PoP_L+PoP_T, mm)

- 1.4
- 1.2
- 1.0
- 0.9

Y2011
- 0.5mm TBP
- 4L PPG
- Low CTE
- 150um BP, LF
- Bare Die PoP
- MLP PoP
- CUF
- EPS

Y2012
- 0.5~0.4mm TBP
- 4L PPG, 6L ABF
- Low CTE/ UL CTE
- 150um BP, LF Solder
- 108um BP, Cu column
- MLP PoP, MUF

Y2013
- 0.4~0.35mm TBP
- 4L PPG, 6L ABF
- UL CTE
- MLP ED, MUF
- Cu col. MR/ TCNCP
- Bare Die PoP
- Pre-Stack

Y2014 ~ 2015
- 0.3mm TBP
- MR/TCNCP
- Interposer PoP
- Plated Cu Post

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INEMI Workshop on Board Assembly & Test Technology, Shenzhen, China, Aug. 25-26, 2014
### PoP FC Interconnect & Substrate Technology Trends

<table>
<thead>
<tr>
<th>Max Height</th>
<th>0.82mm</th>
<th>0.70mm</th>
<th>0.67mm</th>
<th>0.62mm</th>
<th>0.59mm</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Thinner Pop</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bump Pitch</td>
<td>150um</td>
<td>120um - 60um</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interconnect</td>
<td>Solder Bump</td>
<td>Cu Column/ fcCuBE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bonding</td>
<td>Mass Reflow (MR)</td>
<td>MR or TCB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Collapsed B. Height</td>
<td>70- 60 um</td>
<td>45- 30 um</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Substrate Tech.

- 6L, 100um core/ 35um PPG/ 370um thick
- 6L, 150um core/ 25um ABF/ 380um thick
- ULCTE core (3-4 ppm/C)
- Surface Finish: Cu OSP+SOP, Cu OSP
- 6L ,100um core/ 25um PPG. 290um thick
- 6L,150um core/ 15um ABF, 300um thick
- Super Low CTE, Asymmetric PPG, Low RC
- Surface Finish: Ni/Au, Thin Ni ENEPIG, IT
- SMD
- NSMD, ST Trench, Full Open SR
### SCL fcPoP Technology Leadership & HVM Experience

#### PoP Package Technology

<table>
<thead>
<tr>
<th></th>
<th>Bare Die PoP</th>
<th>MLP PoP</th>
<th>MLP PoP - Exposed Die (ED)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HVM</td>
<td>HVM Since 2009</td>
<td>HVM Since 2010</td>
<td>HVM 2013</td>
</tr>
</tbody>
</table>

#### fc-PoP Package Tech Trends & Drivers

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>High-End</td>
<td>MLP PoP-ED</td>
<td>MLP PoP-ED</td>
<td>MUF</td>
</tr>
<tr>
<td></td>
<td>BD PoP</td>
<td>interposer PoP</td>
<td>Advanced CUF</td>
</tr>
<tr>
<td>Drivers</td>
<td>Height Reduction</td>
<td>Improved Warpage</td>
<td>Fine TBP MLP</td>
</tr>
<tr>
<td></td>
<td>Higher MI IO</td>
<td></td>
<td>fcCuBE-MR</td>
</tr>
<tr>
<td></td>
<td>Cost</td>
<td></td>
<td>UL CTE Subs.</td>
</tr>
<tr>
<td>Mid-End</td>
<td>MLP PoP-OM</td>
<td>BD PoP</td>
<td>UL CTE Subs.</td>
</tr>
<tr>
<td></td>
<td>BD PoP</td>
<td></td>
<td>Fine TBP BD PoP</td>
</tr>
<tr>
<td>Drivers</td>
<td>Higher MI IO (0.4mm)</td>
<td>Higher MI IO (0.4mm)</td>
<td>Advanced CUF</td>
</tr>
<tr>
<td></td>
<td>Cost</td>
<td>Cost</td>
<td>fcCuBE-MR&lt;100/50um BP</td>
</tr>
<tr>
<td>Low-End</td>
<td>BD PoP</td>
<td>BD PoP</td>
<td>UL CTE Subs.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>fcCuBE-MR 100/50um BP</td>
</tr>
<tr>
<td>Drivers</td>
<td>Cost</td>
<td>Cost</td>
<td></td>
</tr>
</tbody>
</table>
## PoP Trends & Market Segmentation

<table>
<thead>
<tr>
<th></th>
<th>2010</th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>High-Tier</strong></td>
<td><img src="image1.png" alt="Image" /></td>
<td><img src="image2.png" alt="Image" /></td>
<td><img src="image3.png" alt="Image" /></td>
<td><img src="image4.png" alt="Image" /></td>
<td><img src="image5.png" alt="Image" /></td>
<td><img src="image6.png" alt="Image" /></td>
</tr>
<tr>
<td></td>
<td>14x14 mm</td>
<td>14x14 mm</td>
<td>14x14 mm</td>
<td>14x14 mm</td>
<td>14 - 15 mm</td>
<td>14 - 15 mm</td>
</tr>
<tr>
<td></td>
<td>0.5mm TBP</td>
<td>0.5mm TBP</td>
<td>0.5 - 0.4 TBP</td>
<td>0.5 - 0.3 TBP</td>
<td>0.5 - 0.3 TBP</td>
<td>0.5 - 0.3 TBP</td>
</tr>
<tr>
<td></td>
<td>LF Bump</td>
<td>LF Bump</td>
<td>LF Bump</td>
<td>LF &amp; Cu Bump</td>
<td>LF &amp; Cu Bump</td>
<td>LF &amp; Cu Bump</td>
</tr>
<tr>
<td></td>
<td>4L PPG</td>
<td>4L - 6L PPG</td>
<td>4L - 6L PPG</td>
<td>4L - 6L PPG, 6L ABF</td>
<td>4L - 6L PPG, 6L ABF</td>
<td>4L - 6L PPG, 6L ABF</td>
</tr>
<tr>
<td><strong>Mid-Tier</strong></td>
<td><img src="image7.png" alt="Image" /></td>
<td><img src="image8.png" alt="Image" /></td>
<td><img src="image9.png" alt="Image" /></td>
<td><img src="image10.png" alt="Image" /></td>
<td><img src="image11.png" alt="Image" /></td>
<td><img src="image12.png" alt="Image" /></td>
</tr>
<tr>
<td></td>
<td>14x14 mm</td>
<td>14x14 mm</td>
<td>14x14 mm</td>
<td>14 - 15 mm</td>
<td>14 - 15 mm</td>
<td>14 - 15 mm</td>
</tr>
<tr>
<td></td>
<td>0.5mm TBP</td>
<td>0.5mm TBP</td>
<td>0.5 - 0.4 TBP</td>
<td>0.4 TBP</td>
<td>0.4 TBP</td>
<td>0.4 TBP</td>
</tr>
<tr>
<td></td>
<td>LF Bump</td>
<td>LF Bump</td>
<td>LF Bump</td>
<td>LF &amp; Cu Bump</td>
<td>LF &amp; Cu Bump</td>
<td>LF &amp; Cu Bump</td>
</tr>
<tr>
<td></td>
<td>4L PPG</td>
<td>4L PPG</td>
<td>4L PPG</td>
<td>4L - 6L PPG</td>
<td>4L - 6L PPG</td>
<td>4L - 6L PPG</td>
</tr>
<tr>
<td><strong>Low-Tier</strong></td>
<td><img src="image13.png" alt="Image" /></td>
<td><img src="image14.png" alt="Image" /></td>
<td><img src="image15.png" alt="Image" /></td>
<td><img src="image16.png" alt="Image" /></td>
<td><img src="image17.png" alt="Image" /></td>
<td><img src="image18.png" alt="Image" /></td>
</tr>
<tr>
<td></td>
<td>12x12 mm</td>
<td>12x12 mm</td>
<td>12 - 14mm</td>
<td>12 - 14mm</td>
<td>12 - 14mm</td>
<td>12 - 14mm</td>
</tr>
<tr>
<td></td>
<td>0.5mm TBP</td>
<td>0.5mm TBP</td>
<td>0.5 - 0.4 TBP</td>
<td>0.5 - 0.4 TBP</td>
<td>0.5 - 0.4 TBP</td>
<td>0.5 - 0.4 TBP</td>
</tr>
<tr>
<td></td>
<td>4L PPG</td>
<td>4L PPG</td>
<td>4L - 6L PPG</td>
<td>4L - 6L PPG</td>
<td>4L - 6L PPG</td>
<td>4L - 6L PPG</td>
</tr>
<tr>
<td></td>
<td>LF Bump</td>
<td>LF Bump</td>
<td>LF Bump</td>
<td>LF &amp; Cu Bump</td>
<td>LF &amp; Cu Bump</td>
<td>LF &amp; Cu Bump</td>
</tr>
</tbody>
</table>

INEMI Workshop on Board Assembly & Test Technology, Shenzhen, China, Aug. 25-26, 2014
fcCuBE Bare Die fcPoP - 12x12mm, 0.4mm TBP

PoPb only:

<table>
<thead>
<tr>
<th>Lot</th>
<th>Wafer</th>
<th>Substrate</th>
<th>Ass’y yield</th>
<th>Copl (ave/max)</th>
<th>Warpage (ave/max)</th>
<th>Reliability at SCK Lab</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Input Qt’y</td>
<td>Output Qt’y</td>
<td>Before Bake</td>
<td>After Bake</td>
</tr>
<tr>
<td>Lot1</td>
<td>&lt;100 um</td>
<td>A-Supplier</td>
<td>135</td>
<td>135</td>
<td>100%</td>
<td>61/72</td>
</tr>
<tr>
<td>Lot2</td>
<td></td>
<td></td>
<td>135</td>
<td>135</td>
<td>100%</td>
<td>62/72</td>
</tr>
<tr>
<td>Lot3</td>
<td></td>
<td></td>
<td>135</td>
<td>135</td>
<td>100%</td>
<td>61/74</td>
</tr>
</tbody>
</table>

Stack-up:

Key development project w/ both MR & TCFC w/ leading mobile customer

- Bare die PoP with 0.40mm TBP enabled by the use of Cu column / fcCuBE
- Passed REL with 32nm ELK Si
Height Reduction, MLP ED, 0.3mm TBP

• **Overview:**
  - MLP ED down to 0.3mm TBP
  - Existing infrastructure & process flow
  - Enables PoP pre-stack height of 1.00mm, max

• **Considerations:**
  - Warpage & co-planarity are the main challenges

• **Current Status:**
  - 0.35mm TBP proven and meets 1.00 mm max height
  - 0.3mm TBP will utilize 140um mold cap, 0.17mm top SB, Supplier pre-applied
### Interposer PoP

- Interposer PoP utilizing plated Cu or LF solder
- Scalable to less than 0.3mm TBP
- With TCFC or MR process

<table>
<thead>
<tr>
<th>Option #</th>
<th>Package Description/ Type</th>
<th>FC Bonding</th>
<th>Process / Features</th>
<th>Considerations</th>
<th>Package H. max</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Cu Post Interposer MLP PoP</td>
<td><img src="image" alt="Image" /></td>
<td>Conventional MLP PoP- ED&lt;br&gt;Mass Reflow</td>
<td>Area array PoP&lt;br&gt;Unit based interposer attach&lt;br&gt;Warpage issues</td>
<td>0.70mm</td>
</tr>
<tr>
<td>2</td>
<td>Cu Post Interposer PoP</td>
<td><img src="image" alt="Image" /></td>
<td>FAM&lt;br&gt;No Laser Ablation&lt;br&gt;Mass Reflow</td>
<td>Area array PoP&lt;br&gt;Better warpage control&lt;br&gt;Requires strip based interposer attach/ yield?</td>
<td>0.58mm</td>
</tr>
<tr>
<td>3</td>
<td>CCSB Interposer MLP PoP</td>
<td><img src="image" alt="Image" /></td>
<td>FAM&lt;br&gt;No Laser Ablation&lt;br&gt;TCNC</td>
<td></td>
<td>0.56mm</td>
</tr>
<tr>
<td>4</td>
<td>Interposer Ring PoP</td>
<td><img src="image" alt="Image" /></td>
<td>Conventional MLP PoP&lt;br&gt;CCSB&lt;br&gt;Interposer Attach</td>
<td>Area array PoP&lt;br&gt;Unit based interposer attach&lt;br&gt;Warpage issues</td>
<td>0.70mm</td>
</tr>
<tr>
<td>5</td>
<td>Cavity Interposer PoP</td>
<td><img src="image" alt="Image" /></td>
<td>FAM&lt;br&gt;No Laser Ablation&lt;br&gt;Mass Reflow</td>
<td>Peripheral array PoP&lt;br&gt;Strip based interposer attach&lt;br&gt;Improved warpage</td>
<td>0.50mm</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td><img src="image" alt="Image" /></td>
<td>FAM&lt;br&gt;No Laser Ablation&lt;br&gt;Mass Reflow</td>
<td></td>
<td>0.55mm</td>
</tr>
</tbody>
</table>
4. Fan-out wafer-level package on package (eWLB-PoP) experiences
Fan-out WLP/ eWLB Products Portfolio

- Comprehensive portfolio of Fan-out Wafer Level Packaging (WLP) solutions
- Versatile platform for 2D, 2.5D and 3D integration that delivers significant performance, size and cost benefits

<table>
<thead>
<tr>
<th>3D below 0.6mm</th>
<th>3D eWLB (2S)</th>
<th>3D Face-to-Face (2S)</th>
<th>eWLB-PoP (1.5S)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>package or die</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>2.5D</th>
<th>2.5D / Extended eWLB</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>2D below 0.4mm</th>
<th>Single chip eWLB</th>
<th>Multi-chip eWLB</th>
<th>Flip Chip eWLB</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

eWLL
STATS ChipPAC Delivers Industry Leading Ultra Thin Package-on-Package Solutions with eWLB Packaging

Recent advances in embedded wafer level packaging technology reduce bottom package height to less than 0.3mm for an overall PoP stack height as low as 0.8mm.

Singapore - 20 August 2013 - STATS ChipPAC Ltd. (“STATS ChipPAC” or the “Company” - SGX-ST: STATSChP), a leading provider of advanced semiconductor packaging and test services, today announced a new milestone in reducing Package-on-Package (PoP) height with its ultra thin embedded Wafer Level Ball Grid Array (eWLB) technology. STATS ChipPAC has pursued innovative advances in embedded packaging design methodology, process enhancements and cost structure to deliver eWLB-based PoP solutions with an ultra thin package profile height of 0.3mm.
eWLB Ultra Thin Package on Package Attributes

- PoP packages larger than 15x15mm have been enabled using eWLB HVM processes
- Ultra Thin <400μm total bottom package thickness with embedded high density vias
- Package successfully passed all Component Level and Board Level Reliability Tests
- 2L RDL standard (3L RDL optional)
- Laser formed top via opening
- Top ball pitch comes down to 0.2mm (~ 1000 I/O in 14x14mm PKG)
- Pre-stacked assembly option available for top package
- Ready for HVM today!
### 1.5S eWLB-PoP Stackup

**Package Configuration**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die Size (designed)</td>
<td>~11mm x 11mm</td>
</tr>
<tr>
<td>PKG Size (designed)</td>
<td>~16mm x 16mm</td>
</tr>
<tr>
<td>Ball Composition</td>
<td>SAC305</td>
</tr>
<tr>
<td>Min. TBP</td>
<td>200um</td>
</tr>
<tr>
<td>3D PCB Component Thickness</td>
<td>140um</td>
</tr>
<tr>
<td>Die Thickness</td>
<td>150um</td>
</tr>
<tr>
<td>RDL Stack thickness</td>
<td>50um</td>
</tr>
<tr>
<td>Package ball height/size</td>
<td>110um</td>
</tr>
<tr>
<td>H, PKG Total Thickness (nominal)</td>
<td>310um</td>
</tr>
</tbody>
</table>

**eWLB Process Flow:**

1. Lamination of foil onto carrier
2. Chip placement
3. Molding
4. De-bonding of carrier

- Silicon wafer BG
- Silicon wafer dicing
- Reconstitution
- Redistribution
- Ball Drop / Reflow
- Panel Probe
- Back Grind (Optional)
- Laser Marking
- Package Singulation
- Package Pick & Place
- Ship in TnR
## Final PoPb Structure with 2L RDL / 0.3mm Pitch

### Table of Measurements

<table>
<thead>
<tr>
<th>Description</th>
<th>Sym</th>
<th>Nominal</th>
<th>Maximum</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interposer substrate</td>
<td>a</td>
<td>120um</td>
<td>150um</td>
<td></td>
</tr>
<tr>
<td>Interposer adhesive</td>
<td>b</td>
<td>20um</td>
<td>10um</td>
<td>optional</td>
</tr>
<tr>
<td>Die to mold gap</td>
<td>c</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Die thickness</td>
<td>d</td>
<td>200um</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Die bump collapse height</td>
<td>e</td>
<td>NA</td>
<td></td>
<td>55um : die to PPG</td>
</tr>
<tr>
<td>Interposer Cu column height</td>
<td>f</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Top ball collapse height</td>
<td>g</td>
<td>50um</td>
<td></td>
<td>SRO of Interposer/eWLB top :</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>160um</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SB : 130 - 150um</td>
</tr>
<tr>
<td>Mold gap thickness</td>
<td>h</td>
<td>200um</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bottom substrate / RDL</td>
<td>i</td>
<td>40um</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total eWLB body thickness</td>
<td>h + i</td>
<td>240um</td>
<td>265um</td>
<td>SRO : 250um</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SB : 200 - 250um</td>
</tr>
<tr>
<td>Bottom ball collapse height</td>
<td>j</td>
<td>160um</td>
<td>175um</td>
<td></td>
</tr>
<tr>
<td>Total height (Nom)</td>
<td>k</td>
<td>540um</td>
<td>Max. 600um</td>
<td></td>
</tr>
</tbody>
</table>
1.5S eWLB-PoP Component-level Reliability

<table>
<thead>
<tr>
<th>Reliability Test</th>
<th>JEDEC</th>
<th>Test Condition</th>
<th>Read-out</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSL3 + 3x refloows</td>
<td>JESD20-A120</td>
<td>30°C / 60% RH</td>
<td>192hrs</td>
<td>Pass</td>
</tr>
<tr>
<td>Unbiased HAST (W/ MSL3)</td>
<td>JESD22-A118</td>
<td>130°C, 85%RH</td>
<td>168hrs</td>
<td>Pass</td>
</tr>
<tr>
<td>Temperature Cycling (TC-B, w/ MSL3)</td>
<td>JESD22-A104</td>
<td>-55°C/125°C; 2Cy/hr</td>
<td>1000x</td>
<td>Pass</td>
</tr>
<tr>
<td>High Temp. Storage (HTS w/o PC)</td>
<td>JESD22-A103</td>
<td>150°C</td>
<td>1000hr</td>
<td>Pass</td>
</tr>
</tbody>
</table>

eWLB-PoP Board-level Reliability (Stacked PoP)

- **JEDEC DT**
  - No failure after 300 drops with/without underfill (16x14mm eWLB-PoP)

- **JEDEC TCoB (-40/125°C; 8 layer board)**
  - No failure after 950 cycles without underfill (16x14mm, eWLB-PoP)
4L Laminate and 2L eWLB
(design examples for same functions)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Laminate</th>
<th>eWLB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pad Pitch</td>
<td>40um staggered (80um in one row)</td>
<td>40um staggered (80um in one row)</td>
</tr>
<tr>
<td>Signal Trace W/S</td>
<td>30um/30um</td>
<td>10um/10um</td>
</tr>
<tr>
<td>Via Diameter</td>
<td>60um/100 um(in prepage/core)</td>
<td>30um</td>
</tr>
<tr>
<td>Capture Pad</td>
<td>130um/200um</td>
<td>60um</td>
</tr>
<tr>
<td>Via Pad Clearance</td>
<td>50um</td>
<td>10um</td>
</tr>
</tbody>
</table>

- Finer L/S in eWLB allows to implement signal traces in smaller area, to allocate more area for P/G nets
- Via and via pad are 2-3 times smaller in eWLB
- Typically 2-3 times area saving can be made using eWLB routing. This translates to have 2-3 times less layers to implement the same nets with the same package size
The DDR standard requires a minimum +/-100mV signal for logic detection.

The above simulated eye diagrams show excellent signal integrity. These results include simultaneous switching noise and crosstalk for the 10-channel bus.

Higher power-plane capacitance (for decoupling purpose) than in laminate design, which would help to yield a better power integrity performance from eWLB-PoP.
## Thermal Simulation Data of 14x14mm PoPb (eWLB, fcPoP) Comparison

<table>
<thead>
<tr>
<th>Package</th>
<th>Power (W)</th>
<th>$T_A$ (°C)</th>
<th>$T_J$ (°C)</th>
<th>$Q_{JA}$ (°C/W)</th>
<th>$Y_{JT}$ (°C/W)</th>
<th>$Y_{JB}$ (°C/W)</th>
<th>$Q_{JB}$ (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>eWLB-PoP 14x14mm</td>
<td>3</td>
<td>50.0</td>
<td>103.1</td>
<td>17.7</td>
<td>0.01</td>
<td>5.22</td>
<td>5.61</td>
</tr>
<tr>
<td>fcPoP 14x14mm</td>
<td>3</td>
<td>50.0</td>
<td>103.6</td>
<td>17.85</td>
<td>0.05</td>
<td>5.89</td>
<td>6.20</td>
</tr>
</tbody>
</table>

Fig. 1. eWLB version under natural convection and 3W.

Fig. 2: fcPoPb version under natural convection and 3W.
5. Summary
In Summary

- fcCuBE and low cost substrate technology was illustrated driving cost innovation.
- Several advanced fc-PoP (BD, MLP ED/OM, interposer, etc.) was presented to achieve high performance requirement.
- Thinner package height and smaller TBP was utilized in fc-PoP.
- Advanced low profile eWLB-PoP was developed using eWLB (fan out WLP) and MLP technology of laser ablation and solder filling.
- Ultra thin profile PoP solutions with less than 0.8mm PoP structure and over 500 IO top ball interconnects (dev. target: 0.67mm max.).
- The fc-PoP and eWLB-PoP passed JEDEC standard component level reliability and board level reliability tests.
- eWLB-PoP showed good electrical performance and good thermal performance as well. The PoP structure has lower warpage over reflow profile.
- The fc-PoP and eWLB-PoP technology provides more value-add in performance and promises to be a new packaging platform that can expand its application range to various types of mobile/portable devices as well as 3D SiP systems.