IBM Electronic Card Assembly & Test (ECAT) Technology Gap Analysis

Wayne Zhang | Larry Pymento | Matt Kelly | Derek Robertson | Marie Cole
ISC Engineering, Global Execution

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Server Card Assembly Technology Roadmap Elements

- Intent
- Typical Server Assembly Process Flows
- Technology Gap Analysis
  - Assembly Processes
  - Rework Capability
  - Test
  - Temperature Sensitive Components
  - Electronic Component Technologies
  - Printed Circuit Boards
  - Assembly Materials
  - Tool Capability – Production, Inspection & Analysis
  - Other Considerations
    - Design Attributes
    - Board Flexure, Strain, Warpage
    - PCB
- Summary
Intent

- Assure highest quality and reliability for IBM server hardware, while engaging with contract manufacturing (CM) partners and industry consortia
- Communicate IBM view of server electronic card assembly and test trends
- Ensure industry develops necessary capabilities and competence
- Help close identified technology capability gaps through development projects moving forward
Typical ECAT Lead-Free Thermal Assembly Process Exposures

Typical process flows used across IBM WW manufacturing locations

**Low / Med Complexity Assemblies**
- Card Thickness range: 0.062” – 0.110”
- Card x/y Dimension range: 6”x4” – 15”x17”
- Assembly fixturing required: SMT & PTH pallets
- Typical IBM hardware examples: x/pServer, Storage cards

![Diagram of process flows]

- SMT Bottom Side Convection Reflow
- SMT Top Side Convection Reflow
- PTH Primary Attach Wave Soldering
- Compliant Pin Attachment
- Rework: Hand iron Hot Gas Solder Fountain Compliant Pin
- Back-end processing

**Med / High Complexity Assemblies**
- Card Thickness range: 0.110” – 0.130”
- Card x/y Dimension range: 8”x10” – 18”x20”
- Assembly fixturing required: SMT & PTH pallets, minimal load head fixtures
- Typical IBM hardware examples: x/p/zServer

![Diagram of process flows]

- SMT Bottom Side Convection Reflow
- SMT Top Side Convection Reflow
- PTH Primary Attach Wave Soldering
- Compliant Pin Attachment
- Rework: Hand iron Hot Gas Solder Fountain Compliant Pin
- Back-end processing

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**High / Ultra High Complexity Assemblies**

Card Thickness range: 0.120” – 0.240”
Card x/y Dimension range: 16”x18” – 18”x24”
Assembly fixturing required: SMT & PTH pallets, multiple load head fixtures
Typical IBM hardware examples: p/z HE Server

- **SMT Bottom Side Convection Reflow**
- **SMT Top Side HHH Convection Reflow**
- **Compliant Pin Attachment**
- **Rework:**
  - Hand iron Hot Gas LVP Solder Fountain Compliant Pin
- **Back-end processing**

<table>
<thead>
<tr>
<th>Temperature Range</th>
<th>Notes</th>
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<tbody>
<tr>
<td>10-15C ΔT 245C Max peak 245C 70-140sec</td>
<td>TALs</td>
</tr>
<tr>
<td>10-20C ΔT 245+ Max peak 245+ 90-300sec</td>
<td>Typically no thermal exposures/CP only past 0.120”/no PTH past 0.120”</td>
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<tr>
<td>Variety of temps &amp; TALS Temps can see 260C</td>
<td>Complex LGA attach Advanced mech attach</td>
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**Typical IBM hardware examples:** p/z HE Server

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**High / Ultra High Complexity Assemblies**

Card Thickness range: 0.120” – 0.240”
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Assembly fixturing required: SMT & PTH pallets, multiple load head fixtures
Typical IBM hardware examples: p/z HE Server

- **SMT Bottom Side Convection Reflow**
- **SMT Top Side Vapor Phase Reflow**
- **Compliant Pin Attachment**
- **Rework:**
  - Hand iron Hot Gas LVP Solder Fountain Compliant Pin
- **Back-end processing**

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<td>1-2C ΔT 240 Max peak 240 90-300sec</td>
<td>Typically no thermal exposures/CP only past 0.120”/No PTH past 0.120”</td>
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Assembly Processes

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<tbody>
<tr>
<td>1</td>
<td>Wave Soldering large (ex. 22 inch wide) and thick assemblies</td>
<td>New equipment and process development needed</td>
<td>120mil+ then convert to CP, but still a need for 150mil waver solder applications (niche) Automated selective soldering capability for low PTH counts component tailstock limit of 140 mils; limits protrusion Increasing number of heavy copper power planes (4+, 2 to 3 oz copper) Increasingly designing out of wave solder components for thicker boards</td>
</tr>
</tbody>
</table>

- Other assembly process challenges to consider
  - Paste volume control with increased diversity of feature sizes
  - Cleanliness, workmanship and handling
  - High resolution temperature profiling
### Rework Capability

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<tr>
<td>1</td>
<td>Back to Back Array devices (BGA, QFN’s, Solder charge, DIMM’s etc)</td>
<td>Process development needed for large BGAs and DIMMs.</td>
<td>Mirrored constructions Use of trigger thermocouples – improved process control</td>
</tr>
<tr>
<td>2</td>
<td>Multiple rework site capability</td>
<td>New nozzle designs and process optimization needed.</td>
<td>New processes/special nozzles to increase rework sites</td>
</tr>
</tbody>
</table>

- Other rework capability challenges to consider
  - Long components (SMT DIMMs) with tight spacing and/or neighboring components
  - PTH components (selective rework): pre-heat equipment, optimized contact time
  - Large body BGA, HLGA components on thick boards (>0.130”)
  - Rework of components within a cavity (ex: passives in HLGA socket)
  - Rework workmanship verification
### Test

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| 1    | ICT Contact Issue  | • Define and validate a solder application process or develop new probe contact.  
• Evaluate a selective plating process for test points (over OSP), up to 8 mil FHS | Side effects of OSP surface finishes can lead to contact problems, affecting yields and test throughput. Methods for improving contact performance need to be evaluated. |

- Other test challenges to consider
  - ICT tester capabilities for >10k nets
  - Bead probe test points
Temperature Sensitive Components

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<tr>
<td>1</td>
<td>TSC identification, monitoring, and control</td>
<td>Systematic data and process approach needs to be developed at CMs.</td>
<td>Critical components: electrolytic capacitors, board mounted power (BMP) regulators, LEDs. Require CMs to develop internal database records for part numbers /AVLs, with updates / maintenance; 20+ channel thermocouple monitoring / datalogger requirement</td>
</tr>
<tr>
<td>2</td>
<td>Design for Temperature Sensitivity (Increased Process Windows)</td>
<td>ODM / JDM partner needs to develop TSC management methodology</td>
<td>ODM/JDM projects depend on internal records/database for part selection</td>
</tr>
</tbody>
</table>

- Other temperature sensitive component challenges to consider
  - Understanding of temperature sensitive component issue and J-STD-075 (HDP User Group project)
  - Complex thermal shielding
  - Design for reliability (part selection)
Electronic Component Technologies

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<tr>
<td>1</td>
<td>HLGA Sockets</td>
<td>Process optimization and verification needed for &gt;3200 I/O or &gt;65mm</td>
<td>2190 I/O 50mm (standard) / 3000 I/O 55x65mm / 3777 I/O 68.5mm². 4 sockets per card 2 piece CPU socket designs (75 mm x 62.5 mm) varied pitch, pad definitions, &gt; 3,300+ I/O Drives need for HIP resistant solder paste selection Loading, forces, thermal solution / hardware footprints Site flatness after reflow -&gt; Cu aprons/tighter coplanarity control/PCB flatness 3,777 I/O Hybrid LGA required to meet max warpage 5.5mils(0.14mm) @ 265°C Rework profiles/equipment for thick, multi-plane socketed PCBA's</td>
</tr>
<tr>
<td>2</td>
<td>Compliant Pin Interconnect</td>
<td>Process development and verification needed for micro-compliant pin and double sided designs</td>
<td>Micro-compliant pin designs Double sided compliant pin applications Adjacent thermal rework drives pin retention concerns Use with back drilled PTH via definitions</td>
</tr>
<tr>
<td>3</td>
<td>Solder charge SMT connectors</td>
<td>Process development and verification needed</td>
<td>Eg. Neoscale, SeaRay, in single side and dual sided-mirror footprint layout</td>
</tr>
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</table>

- Other electronic component challenges to consider
  - Anti-sulfur resistors (ASRs) or other corrosive environment mitigation (conformal coating)
  - Fine pitch (0.5 / 0.3mm) BGAs and CSP
  - Multi-row QFNs
  - SMT DIMMs with light pipes or fork locks
## Assembly Materials

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<tr>
<td>1</td>
<td>Solder Preforms</td>
<td>SMT process dev&lt;br&gt; Evaluation of paste-in-hole benefits needed; validation of component compatibility.</td>
<td>Increased capability for niche applications (SMT – ex. oscillators / FETs)&lt;br&gt;Enhance paste-in-hole fill performance</td>
</tr>
<tr>
<td>2</td>
<td>Low Temperature Alloys</td>
<td>Alloy selection and development needed (some industry projects already in progress for reflow).</td>
<td>Development for PTH wave and solder fountain applications; maximizing hole fill, minimizing Cu dissolution&lt;br&gt;Need substantial Temp reduction to consider use minor temp reductions have little impact on extended TALs</td>
</tr>
<tr>
<td>3</td>
<td>Solder Paste</td>
<td>Evaluations / validations needed for solder pastes in complex assemblies.</td>
<td>HiP Resistance: next generation solder paste w/ increase HiP resistance needed for increasing I/O HLGA sockets&lt;br&gt;Extended TAL time: Longer time above liquidus (&gt;217C) occurring up to 250-300 seconds (primary attach &amp; rework)&lt;br&gt;Void Reduction: continued reduction for QFN thermal pads, small print deposits&lt;br&gt;Improved Release: for small area ratio pad size range 8 to 10 mils, stencil thicknesses 5 or 6 mils type 3 (standard use) and type 4 pastes</td>
</tr>
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- Other assembly materials challenges to consider
  - Flux application control
  - Flux chemistry (WSP) for high voltage applications
  - Material selection, dispense and cure of isolation materials for high voltage applications
  - Atmospheric pollution / corrosion control – conformal coating options
  - High Conductivity Thermal Interface Materials (TIMs)
## Tool Capability – Production, Inspection & Analysis

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<td>1</td>
<td>Enhanced algorithms for HiP detection with in-line X-ray</td>
<td>Improved detection method needed for HiP.</td>
<td>Varying equipment used in the industry. Algorithms not robust enough.</td>
</tr>
<tr>
<td>2</td>
<td>CT Scan X-ray for FA diagnostics</td>
<td>Equipment capability needed or access to third party lab</td>
<td>Increased coverage for PCB and PCBA analysis,</td>
</tr>
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- Other tool capability (production, inspection, analysis) challenges to consider
  - Large panel capability
  - X-ray inspection capacity / capability
  - Large socket placement capability
  - Failure analysis techniques - dye and pry for small or large components
Other Areas Evaluated in Gap Analysis

- **Design for Assembly via Software driven analytic tools**
- **Design Attributes**
  - Component placement densities increasing
    - front and backside
    - pin density > 50 pins/sq inch and 10K+ placements
  - Via definitions and hole fill robustness
- **Board Flexure, Strain, Warpage**
  - Maximum principle strain and max strain rate validation across all assembly and test operations
  - Module / PCB warpage
- **PCB**
  - High temperature laminate materials
  - Thickness / stack up / increased Cu plane weights
  - Blind / buried vias, Via in Pad (VIP) and Via in Pad Plated Over (VIPPO)
  - Selective PCB finish
Summary

- IBM partnering with industry to improve QUALITY

  ✓ Extends to PCBA and Test FPY, Box line assembly and Field Performance (Reliability)

  ✓ Enabled by Technology Readiness prior to Product Design
    - Consortia and other Industry Participation (iNEMI, HDPUG, Universal AREA etc.)
    - Collaboration with key Technology Partners
    - Active test vehicle studies (with product like attributes)
    - Roadmap gap analysis – work efforts (IBM/Other OEM’s)

  ✓ Enabled by DfX knowledge, Equipment, Process maturity, Material selection and sustained operational procedures/workmanship
Thank you. Questions?

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