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ABSTRACT

08:30  Bill Bader, iNEMI CEO
Opening Address:
iNEMI welcomes all participants from worldwide to this important workshop to exchange information and
develop the collaborative activities among the members.

Biography:
Bill Bader joined iNEMI in August 2009 as Chief Executive Officer. He is a 26-year veteran of Intel Corporation,
and he brings to iNEMI a wide range of experience, including factory management for high-volume production,
new product development, hardware and software design and test, and assembly and test technology
development. He also served as Intel’s representative on the iNEMI Technical Committee from 1998 to 2005.
Mr. Bader received his BSEE from the Rochester Institute of Technology (RIT) in Rochester, New York.

09:00 ~ 09:45  Rozalia Beica
CTO
Yole Development

Subject: Current Technologies and Future Developments in Advanced Packaging

Abstract:
Advanced packaging has significantly grown in the last few decades. If historically, most of the processing was
performed at wafer level and supported by flip-chip wafer bumping using electroplated gold and solder bumps,
today the industry is benefiting from a large variety of different packaging technologies and platforms. Besides
flip chip bumping, incorporating more advanced and multiple devices in smaller and more performing packages
can be performed using embedded technologies, redistribution lines, vertically stacking devices using through-
silicon-via interconnect with or without interposers.
One of the most advanced stacking platforms is 3D IC integration. Because of the potential it has in further
driving the evolution of new packages, 3D IC is considered a new paradigm for the semiconductor industry. A
significant amount of work have already been performed in developing each unit processes and integrating
them seamlessly; however, cost as well as other remaining challenges, such as managing thermal budget,
design, testing and infrastructure readiness for collaborative business model, will need to further develop in
order to increase the rate of adoption of TSV based packaging.
In this talk, Yole will provide an overview of the different packaging technologies with focus on 3D packaging,
presenting the industry developments from substrate to device as well as integration. Description of alternative
stacking platforms such as 2.1D and 2.5D will be presented. Technology prospects, challenges, activities at
major players and business models will be addressed.

Biography:
Rozalia Beica is currently the CTO of Yole Development leading Advanced / 3D Packaging and
Semiconductor Manufacturing activities.
Rozalia is an international award winning scientist (2006 R&D 100 Award), with over 60
publications and several patents. For more than 16 years, Rozalia has been involved in the
research, application and strategic marketing of Advanced Packaging and 3D IC technologies,
with global leading responsibilities at materials (Rohm and Haas), equipment (Semitool, Applied
Materials, Lam Research) and device manufacturing (Maxim IC) organizations. She is actively
involved in industry events and committees worldwide (Technical Chair of 3D Packaging committees and
activities at IMAPS DPC, ECTC and ITRS, member of IWLPC, EMPC committees).
Rozalia has a M. Sc. in Chemical Engineering from Polytechnic University “Traian Vuia” (Romania), a M. Sc. in Management of Technology from Kennedy Western University (USA) and a Global Executive MBA from IE Business School (Spain).

09:45 ~ 10:15  Yasumitsu Orii  
Senior manager of IBM Research Tokyo Science & Technology division  
IBM Japan

Subject:  
Challenge of Packaging Technology in the era of Cognitive Computer

Abstract:  
Big Data growth is accelerating as more of the world's activity is expressed digitally. Not only is it increasing in volume, but also in speed, variety and uncertainty. Most data now comes in unstructured forms such as video, images, symbols and natural language - a new computing model is needed in order for businesses to process and make sense of it, and enhance and extend the expertise of humans. Rather than being programmed to anticipate every possible answer or action needed to perform a function or set of tasks, cognitive computing systems are trained using artificial intelligence (AI) and machine learning algorithms to sense, predict, infer and, in some ways, think. To make it into practice, a much faster rate of system performance improvement, such as 4x/2years which is the double of historic trend (2x/2years) to reach exaflop capabilities (100x-1000x over present systems) is required. In order to deliver this increased demand of system-level performance, new technology innovations are required. Today, semiconductor scaling is still driving improved performance, higher power efficiency, and cost reductions for computer systems, but the current scaling technologies are reaching their physical limits. In the coming cognitive computing era, on behalf of the semiconductor scaling approach, emerging high-density packaging technologies will be the key drivers for the growth of computer systems. A cognitive chip consisting of neurosynaptic elements connected in a neural network structure, which vastly differ from the current semiconductor device architectures, will be a key technology for these future cognitive systems.

Biography:  
Yasumitsu Orii received the B.S. in Material Science from the Osaka University, Japan and the Ph.D. from the Osaka University, Japan as well. He is a senior manager of IBM Research Tokyo Science & Technology division and a Senior Technical Staff Member working in 3D Integration. He received Best Paper Award at the 2008 ICEP (International Conference on Electronics Packaging), Outstanding Paper Award at the IMPACT 2011, JIEP Annual Best Paper award in 2011 and IMAPS Sidney J. Stein International Award in 2012. And he was a chair of Technical Program Committee in ICEP 2009 in Kyoto, 2010 in Sapporo and 2011 in Nara responsible for technical program editing and paper selection. He was the general chair of ICEP-IAAC (IMAPS All Asia Conference) 2012 in Tokyo.

10:15 ~ 10:45  Weifeng Liu  
FLEXTRONICS International

Subject:  
Challenges of Organic Substrates from EMS Perspective

Abstract:  
The International Technology Roadmap for Semiconductors (ITRS) and the International Electronic Manufacturing Initiatives (INEMI) have identified a list of challenges and gaps for organic substrates of BGA type packages. Substrate warpage during the reflow process is one of them. Studies show that excessive substrate
warpage can cause a variety of surface mount soldering defects, like head in pillow (HiP). With the proliferation of thin core/coreless substrates, die and package stacking, fine pitch and lead free reflow, substrate warpage becomes even more challenging and needs to be fully addressed, as this will impact assembly yield, product quality and long term reliability. Although JEDEC has issued publications to define the maximum substrate warpage, package suppliers may not necessarily follow the guidelines. A clear boundary on package substrate warpage is not well defined with strong data support, and many impacting factors are still not well studied and documented. To minimize warpage, package substrate makers tend to design the substrates with low CTE materials, however, this will inevitably impact the second level solder joint reliability. Collaboration between package and substrate suppliers, OEMs and EMSs is needed to address these challenges.

Biography:
Weifeng Liu received the Ph.D. in Mechanical Engineering from University of Maryland at College Park. He is now with the Advanced Engineering Group of Flextronics at Milpitas California, leading the technology development in microelectronics packaging, wearable and printed electronics. Prior to joining Flextronics, he worked at system OEMs (Hewlett Package USA and Huawei China), developing packaging and assembly solutions for system applications. His expertise lies in the areas of microelectronic packaging, assembly and reliability evaluation. He has published dozens of technical papers, holds three US patents and has many pending.

11:00 ~ 11:30 Kinya Ichikawa
Assembly Technology Development-Japan Manager
Technology & Manufacturing Group-Japan
Intel K.K.

Subject:
Key Technology Challenges in Computing Package and Assembly

Abstract:
Computing is moving beyond the PC into a wide range of “smart” devices, driven by the ubiquitous Internet and the ability to be always connected. The compute continuum ecosystem consists of an array of computing devices from the smallest smartphone to the largest cloud server. These new markets have expanded integrated circuit packaging challenges in several areas including electrical, mechanical and thermal performance, form factor (height and area), and cost. Both the industrial and the academic community continue to develop more advanced semiconductor packaging technologies that continue to enable progress and growth in the evolution of computing continuum. This presentation talks about the technological trends and drivers of advanced packaging research, and discusses the challenges and opportunities driven by application specific requirements. The first level interconnect (chip to package) and the second level interconnect (package to board) pitch scaling are the essential to decrease the gap with the relentless silicon technology scaling. Increasing bandwidth density within the package drives innovation including logic and memory interconnects with 2.5D and 3D integration. System densification drives innovations in wafer level packaging to enable further reduction in cost, size and power. Meeting the push for ultra-thin form factors will require advances in thin wafer handling, thin die assembly, thin substrate manufacturing, and package warpage controls. The objective of this presentation is to communicate industry challenges and to encourage the audience to engage in collaborative development efforts to solve these issues.

Biography:
Kinya Ichikawa is a department manager of Assembly Technology Development Japan at Intel K.K. in Tsukuba, Japan. His group represents the new assembly process & equipment technology Pathfinding in Asia. Kinya has been with Intel since 1993 and have had various packaging Pathfinding projects including C4 organic package
discovery. He holds 14 US patents in the field of advanced package solutions, and has published 27 technical papers. He is a member of JIEP and the ICEP technical paper committee. His e-mail is kinya.ichikawa at intel.com.

Subject:
Trends and challenges of electronic packaging for Huawei

Abstract:
With the development and rapid spread of smart terminal product, telecommunications field are facing and experiencing a data storm, from access network, wireless, transmission and switch network, they are all facing the challenge of the network bandwidth bottlenecks, electronic packaging technology endure a huge pressure on low-cost, high-power dissipation, and high-density, a variety of new materials, new packaging technology are required, such as 2.5D/3D packaging, photoelectric integrated, and other high-frequency packaging technology, there are several case in this article to explain the challenge,;
For the IP cluster and data center product, with the bandwidth increase between the component, board and rack, the application of TSV are more closer, but some challenge on the thermal, reliability, infrastructure issue need to be handle; And the optical interconnect application spread from the rack level to board level and component level, such as the high accuracy and efficiency alignment technology should be study to lower down the optical component cost.
For the wireless product, high frequency means the high bandwidth, and also means the consistency and accuracy control for the packaging, it will become difficult to choose the substrate and package structure, and also the supply chain are difficult for this kind of product, hybrid assembly design and some advanced material study are the main method to improve the system performance.

Biography:

Subject:
Perspective from OEM (TBD)

Abstract:

Biography:

Subject:
iNEMI Roadmap Highlight and Technology Gap (tentative)

Abstract:

Biography:
13:40 – 14:05  Assembly & Test Technology  (TBD)

Subject:

Abstract:

Biography:

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Subject:
3D package technologies review with gap analysis for mobile application requirements

Abstract:
3D package technologies with Flip chip, Wafer level and TSV technologies are key and critical to contribute miniaturizations and cost performances of semiconductor products in mobile products like Smart phones and Tablets. The latest technologies and roadmaps are reviewed with gap analysis for application requirements. Flip chip technologies are categorized with bumping types, interconnection processes, under fill types to cover the various requirements. Fan out wafer level packages are going to cover the current FCCSP and FBGA technology areas with better electrical, thermal and structural performances. TSV realizes wider width with better power consumptions which is really requires improving the mobile application performance. This presentation intends to review and analyze the gap between the latest those technologies vs application requirements and propose the approaches to fill the gaps.

Biography:
Flip chip and build up substrate development, application engineering in IBM (1988 – 2010)
Business development in STATS ChipPAC Japan (2010- 2012)
Representative in STATS ChipPAC Japan (2013 - )

14:40 ~ 15:05  Takashi Kariya

Division Manager / R&D Operation, Electronics Development Division
Ibiden

Subject:
Expectation of Embedded Device Technology and Key Challenging Area

Abstract:
In recent years, the embedded active/passive technology is widely attracted for down-sizing mobile products and improving its electrical performance. The package substrate using the technology is now in volume production level, and applied for the advanced mobile product. In this study, the representative embedded substrate technologies are presented by introducing our three developed technologies using the robust structure of the plating connection to satisfy the reliability requirement from our customers.

The three embedded substrate technologies are;
(1) Embedded thinner MLCC in FC-CSP for higher clock frequency and lower power consumption
(2) Embedded Thin Film Capacitor in FC-PKG for high power delivery performance of server application
(3) Embedded active device technology to minimize body size that contribute to control the body warpage by maximizing silicon / body area ratio
For more market expansion of the embedded substrate, we need the improvements for the following three points of view.

1. Technical point: We need to improve the process yield of the embedded substrate manufacturing especially for active device embedded. The embedded substrate routing design correlates to the signal I/O count of the active device. The routing design has to be optimized for minimizing the yield loss by the compensation of active device to be embedded.

2. Cost point: We need more cost saving solution. The embedded substrate cost need to be minimized by optimizing the balance of embedded device area in the substrate, since the no embedded device area is counted the same process cost as the embedded area.

3. Business model point: The business model has to be established for that both substrate and embedded device supplier can agree. The substrate supplier needs embedded device supplier to guarantee the device quality, also needs testing information from embedded device supplier for the sufficient product yield. The collaboration work between substrate supplier and embedded device supplier is essential for the embedded device design and testing especially for establishing the business model.

**Biography:**
Education: Nagoya Institute of technology
Experience: Managing R&D division more than 5 years in Ibiden for advanced FCPKG substrate / FCCSP substrate / Printed Wiring Board / 2.5D-3D SiP / Embedded Passive and Active.

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**Subject:**
The Requirements of Future IC Substrate, a maker point of view

**Abstract:**
Semiconductor technology is moving rapidly from 28nm to 20nm and even 16nm node. Traditional laminate substrate is been challenged to meet the fine line and performance requirement of the IC chips. For future high performance products, fine line such as 5/5 and 3/3 even 2/2 um are required. To meet the challenges, laminate materials with low CTE, low loss and fine line capabilities are required. New substrate requirement such as embedding passive and active components into the substrate is also emerging. Alternative substrate approaches such as 2.5D silicon/glass interposer and 2.1D substrate are proposed to meet the future fine line and fine via requirement.

In this talk, the laminate substrate industry efforts to meet the challenges will be reviewed and new approaches to the fine line of IC substrate will be discussed.

**Biography:**
Dr. Dyi-Chung Hu has a Ph. D. degree from MIT in Material Science and Engineering Department in 1984. He joined IBM East Fishkill to develop thin film substrate for multi-chip modules. On 1990, he went back to Taiwan and become Professor in National Chao Tung University. Later, he joined Industry Research Organization (ITRI) in Taiwan and start development of wafer bumping, TAB and COG process etc. He is one of the pioneers in developing Taiwan TFT LCD industry and he is also the cofounder of two Taiwanese TFT LCD Companies, E-ink and Hannstar. Currently he is a Senior VP in Unimicron and is responsible for advanced substrate and new business development. Dr. Hu has extensive RD development and contributions in the field of semiconductor packaging, Flat Panel display and Advance IC substrate.
Shoji Watanabe
Shinko Electronics Co., Ltd.

Subject:
Development of Organic Multi Chip Package for High Performance Application

Abstract:
Today’s 2.5D packaging technology for high density, high performance interconnect applications is enabled by silicon interposers because of its sub micron line and space capabilities. A possible alternative to silicon is an organic interposer, which offers lower cost, larger sizes, a known manufacturing process. However, it is difficult for conventional laminate build-up technology to achieve better high density wiring, small diameter vias, and dense flip chip bump pads.
In order to meet these requirements, we are developing an Organic Multi Chip Package that integrates organic interposer with a conventional organic substrate.
Our Organic Multi Chip Package is the elimination of attaching a separate standalone interposer onto an organic substrate because the interposer is built directly onto the substrate during processing. Moreover, conventional assembly processes can be used for die assembly onto the substrate.
We demonstrated Organic Multi Chip Package that is the organic interposer integrated with conventional organic substrate. First normal build-up layers are laminated on both sides of the organic core. Then the surface of the final top build-up layer is smoothed by CMP (Chemical Mechanical Polishing) to accept the first thin film dielectric layer of the organic interposer layer. Small diameter vias are opened using photolithography processes, followed by sputtering a metal seed layer for forming the fine metal lines/spaces as 2µm/2µm and for the array of flip chip bonding pads at 40µm pitch. We also demonstrated reliability of this package.

Biography:
He received the B.E. degrees in mechanical engineering from Kanagawa Institute of Technology, Kanagawa, Japan, in 1991. He joined SHINKO ELECTRIC INDUSTRIES CO., LTD., Nagano, Japan, in 1991, where he is engaged in the research and development on advanced package. He is currently involved in developing Organic Multi Chip Package.

Hikari Murai
General Manager
Tsukuba Research Laboratory, Telecommunication Materials Development Center
Hitachi Chemical Co., Ltd.

Subject:
Can we prepare organic materials for 2.1D next generation interposers?

Abstract:
Along with demands of big data and high speed communication, there become higher I/O numbers in one die about high accumulated semiconductor chips. That time it requires the interposer should correspond narrow pitch of bumps and low CTE property as same as chips. Usually silicon interposer selected to above demands, but that is so expensive that the market requests chipper materials instead of silicon. For replace silicon interposer to organic materials, it needs to develop ultra-low CTE core substrate and to make very fine line on organic core by SAP process. In this time we introduce the most advanced core laminates for substrate and challenge for very fine line like less than L/S=5/5. Regarding the core material, we have developed ultra-low CTE core named E-770G applying original resin system with hard segment polymer and soft segment polymer. It achieves the target CTE less than 2ppm/deg C (x,y direction) by TMA method. Also this material has an excellent
reliability and good warpage after mounted chip. About fine line, we developed very unique primer has strong peel strength in spite of flat surface. We succeeded in L/S=5/5 on organic core material using this material.

Biography:
1978 graduated Tokyo Metropolitan University /the department of engineering

17:00 ~ 17:25 Kazuaki Ano
Deputy Senior General Manager, Engineering Division
Shinkawa Ltd.

Subject:
Substrate technology discussions of 2.1/2.5D IC packaging process

Abstract:
The Thermal Compression Bonding (TCB) process is a highlighted technology for fine pitch bonding by using copper pillar with Sn-Ag solder tip. Various resin fill process options, such as NCP, NCF or Capillary Under Fill (CUF), have been evaluated with this process in IDMs and OSATs. Technology driver Si chip has increased I/O counts so it has thousands pillars on its surface hence bonding force becomes higher and higher. By increasing the bond force, lead width on a substrate becomes critical to keep pillar placement accuracy. This is not only substrate issue but mechanical rigidity of bonding head also acts as a cause of bonding accuracy degradation in high force bonding. In this area, bonding machine needs a help to redesign bond leads to solve the degradation. Another aspect of substrate discussion is its thermal expansion during the bond. As long as taking look at the pillar pitch roadmap, 30/60um pitch will be in production in a couple of years. As fact, mismatch on thermal expansion between Si chip and substrate is the critical issue. Recently, low CTE substrate core is introduced but substrate CTE is dominated by copper trace density and its thickness. On the other hands, low temperature solder alloys are introduced and its joint reliability evaluation is ongoing. Anyway, substrate has to overcome those technology gaps in order to be ready for 30/60um pillar pitch in the near future.

Biography:
About 30 years’ experience of Semiconductor Packaging at a foreign owned company. Have been leading packaging technology with a wealth of expertise for FC process, CSP and Cu wire implementation. Work at Shinkawa Ltd, for Jisso development and Advanced Assembly Equipment Development since April 2013.

17:30 ~ 17:55 Haruo Shimamoto
3DIC Study Group Co-Leader/ SEMI Japan

Subject:
3D-IC standardization activity in Japan

Abstract:
1. A background and the need of Standardization
Development of three-dimensional semiconductor integration technology and the device (3D-IC) becomes ready for mass-production all over the world, but horizontal division of manufacturing process in the semiconductor industry restricts the expansion of 3D-IC products. To overcome this situation, informations of manufacturing process, device design rule and quality control points should be correctly transmitted between supply chains. So the standardization activity is indispensable. Particularly, the standardization of characteristic models (electricity, heat, stress) of TSV is important for 3D-IC design and of Metrology of wafer measurement and/or observation is important for 3D-IC production.
2. Activity in Japan
Of course SEMATECH, SEMI, JEDEC, IEEE has been already promoting the standardization of the contents about 3D-IC, what is significant to make standard in Japan? Many material and equipment suppliers for 3D-IC are already existed in Japan, many emerging technologies and ideas are growing up. But unfortunately, 3D-IC Japanese business players in semiconductor are weak, AIST is promoting new framework for standardization which includes existing SEMI Japan 3D-IC Study Group. Connecting with “Development of Next Generation Smart Device Project” which is entrusted by NEDO, JEITA and SEMI are collaborated. I will introduce in this workshop in more detail.

Biography: